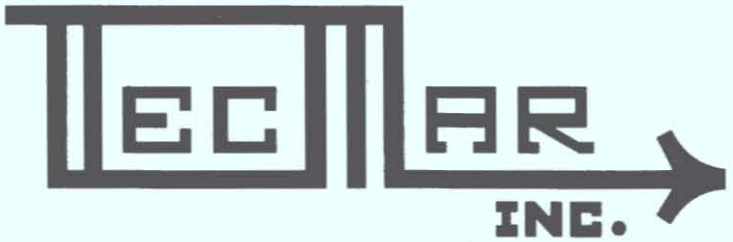

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TM-AD212

S-100 Analog to Digital Converter and Timer/Counter Board

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ERRATA

It is possible that the AD212 board will power up with the AD DONE flag set (=1). If your program uses this flag either for interrupts or status checking, it will be necessary to clear the flag when initializing the board. This can be done simply by reading the high A/D byte which automatically resets the AD DONE flag.

Pins 20, 53, and 70 have been connected to ground per IEEE standard. If your system uses these lines then cut the traces on the board from these lines to ground.

All 14 Bits modules are configured as 16 Bit modules and are left justified. They are actually 16 Bit modules that have fallen out but have at least 14 Bit accuracy.

TECMAR S-100 AD212

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INTRODUCTION

The Tecmar S-100 AD212 board is designed for sophisticated industrial, scientific, commercial, laboratory or educational applications requiring high-speed, accurate analog to digital conversion including real time applications. The AD212 interfaces various Complete Data Acquisition Modules and the AMD 9513 Timer Controller to each other and to the S-100 bus. The AD212 consists of a mother board that plugs into the S-100 bus which has all the control logic and timer circuitry, and a daughter board which has the data acquisition module and the associated jumpering. This daughter board can be plugged into the mother board inside the S-100 bus or connected to the mother board via a ribbon cable. Placing the daughter board outside the S-100 bus is recommended for high gain and/or 14 or 16 bit operation. A separate enclosure is available for the daughter board.

The standard board can be jumpered for 16 single-ended or 8 true differential inputs. Optional expansion boards which accommodate two expansion modules each (48 additional single-ended or 24 additional differential channels per expansion module) provide additional channels up to 256 channels. The standard resolution and accuracy is 12 bits. However, 14 and 16 bit resolution options are available. The higher resolution modules are designed for sophisticated users with very exacting requirements.

The AD212 supports three different modes of programmable gain. The PRK precision resistor kit option provides a selection of seven resistors to achieve gain settings from 1 to 1000. Software programmable gain of each channel is provided by PGH with gains of 1, 2, 4, and 8 for high level inputs or PGL with gains of 1, 10, 100 and 500 for low level, wide range inputs. Single resistor gain programming is not necessary with software programmable gain.

This board complies with the IEEE S-100 specifications and will allow 8 or 16 bit transfer of data. If 8 bit systems are being used, two transfers are necessary. However, if a 16 bit system is being used, only one transfer of data is required. The AD212 automatically recognizes if an 8 or 16 bit device is requesting information so both 8 and 16 bit CPU's can be used in the same system to acquire data from this board. The AD212 may be jumpered to act as an I/O device or memory-mapped device and requires 16 locations.

The data is latched after conversion. This provides the capacity to start the next conversion while reading the information into the computer's memory from the conversion just completed. If the data from the next conversion replaces the data in the latches before the data is read into the computer, a "data overrun" bit is set. The throughput using this technique is comparable to that obtained with direct memory access. The standard module has a conversion rate of 30 KHz. However, options are available for conversion rates of 40 KHz, 100 KHz and 125 KHz.

The A/D can be triggered by an external device. A TTL compatible signal is required. The external trigger signal is under software control. For example, the board could respond to CPU commands which would mask out the external trigger, i.e., the A/D could not respond to the external triggers, and at a later time, under software control, the board could be made to trigger on an external signal. There are also provisions for synchronizing A/Ds enabling the acquisition of data from several sources at the same time.

Auto incrementing from any channel to any channel provides the capability of obtaining data at a specified starting channel and then the next channel, etc. until the specified ending channel is reached at which time it automatically obtains data from the starting channel agian.

Programming directions are thoroughly documented in the technical manual provided with the AD212 and software examples are numerous. The software interfacing techniques available include status bit check, vectored interrupts or CPU suspension.

The AD212 timer is available to the CPU as a general timer, to control A/D conversion, or to interface equipment external to the computer. The timer used is the Am9513. It also has 15 lines available for external use. It contains five independent 16 bit counters which are cascadable and can provide internal timing down to 1 microsecond. It is capable of counting events up to a rate of 7 MHz. Time of day with a resolution to 1 second is available by cascading two timers. There are also alarm comparators on two counters. The Am9513 can be used for continuous frequency outputs or one-shot. It has programmable gating and count source selection.

The Tecmar AD212 Software Support Package (AD212-SSP) is designed to help the user perform complex data acquisition tasks and timing operations with an S-100 computer operating under CP/M and using the Tecmar AD212. The following tasks can be performed with the AD212-SSP:

1. Set time of day
2. Set 24 hour time of day
3. Read time of day
4. Read 24 hour alarm status
5. Collect a given number of data points using the AD212 at a timer interval varying from 40 microseconds to 64 kiloseconds
6. Optional continuous visual monitoring of the data being collected
7. With the TM-DA100 an array of data in memory is converted to an analog signal that can be used to drive a plotter, oscilloscope, etc.
8. An event counter is provided which can count from 0 to 64K
9. A routine is provided which displays the contents of an integer array on a video monitor (see option 6)

The AD212 is designed to meet a wide range of sophisticated data acquisition needs at a low price with high reliability.

AD212 FEATURES

- IEEE S-100
- 16 single-ended or 8 true differential inputs -- jumper selectable
- 12 bit accuracy and resolution standard
- 30 KHz conversion rate standard
- I/O or memory mapped -- switch selectable
- Jumper selectable input ranges: ±10V, ±5V, 0 to +10V, 0 to +5V
- Output formats: two's complement, binary, offset binary
- Transfers data in 8 or 16 bit words
- Provision for expansion to 256 channels
- External trigger of A/D under computer control
- Auto channel incrementing from any channel to any channel
- Utilizes vectored interrupts, status test of A/D or CPU suspension
- Provision for synchronizing A/Ds
- Data is latched providing pipelining for higher throughput
- Data overrun detection
- Includes high-speed sample-and-hold and precision multiplexer
- Power connector provided to supply user's external circuitry
- Thorough documentation including numerous software examples
- No user adjustments

TIMER FEATURES

In addition to the A/D features, the AD212 contains a powerful timer circuit which can start A/D conversion and can also be used independently for time of day, event counting, frequency shift keying and many other applications.

- 5 independent 16 bit counters (cascadable)
- 15 lines available for external use
- Time of day
- Event counter
- Alarm comparators on 2 counters
- One shot or continuous frequency outputs
- Complex duty cycle and frequency shift keying outputs
- Programmable gating and count source selection
- Utilizes vectored interrupt

AD212 OPTIONS

- Programmable gain up to 1000
- 14 bit accuracy
- 16 bit accuracy
- 40 KHz conversion rate
- 100 KHz conversion rate
- 125 KHz conversion rate
- Screw terminal and signal conditioning panel with optional thermocouple cold junction compensation and rack mount enclosure
- Enclosure and cable for remote daughter board
- Low level, wide range (10mV to 10V FSR) permitting low level sensors such as thermocouples, pressure sensors and strain gauges to be directly connected to the module input
- Complete channel to channel isolation up to ±250V with ±250V of common mode range
- Expansion boards for up to 256 channels
- AD212 Software Support Package

AD212 CIRCUIT DESCRIPTION AND SET-UP GUIDE

1. Conventions

Orientation references in the following description such as "up, down", etc. assume that the AD212 is being viewed with its S100 connector (P1) pointing down.

Signals described as being "high" or "low" refer to voltages of 3 to 5 volts or zero volts, respectively. Signals described as being "true" or "false" refer not to voltage levels, but to the relationship between the voltage levels and the presence or absence of "bubbles" (or small circles) where the signal trace on the schematic connects to the circuit element. The absence of a bubble means that "true" is "high" and "false" is "low". The presence of a bubble means that "true" is "low" and "false" is "high".

2. General

The AD212 is constructed out of two printed circuit boards, one of which is called the mother board and the other the daughter board. The mother board contains entirely digital logic and plugs directly into the S100 bus. The daughter board contains all the analog circuitry and is designed to bolt rigidly to the back of the mother board thus creating a single unit which occupies two S100 bus slots. Pin and socket style connectors are used to carry signals between the two boards. Since these are compatible with ribbon cable connectors, it is optionally possible to locate the daughter board at a location remote from the S100 mainframe. This feature has the advantage of allowing the daughter board to be located nearer to the source of the signals being acquired rather than having to run these signals over a distance and into the noisy S100 mainframe which might cause noise pickup. The AD212 is designed to work with as much as about 100 feet of ribbon cable between the two boards although even longer runs may be possible depending on the environment. The daughter board has six standoffs swaged to it that accept 6-32 threaded bolts to facilitate mounting in a remote location.

The AD212 is designed to be totally compatible with the proposed IEEE S100 bus standards. This is, in general, an advantage, but there are specific details in the new standard which are not compatible with some earlier processors. For users of the AD212, the most important potential incompatibility arises from the fact that the AD212 uses all of the proposed, additional ground connections to the S100 bus. These are pins 20, 53 and 70. If any of these bus lines are in use in the machine which the AD212 will be used with, then the corresponding ground traces on the AD212 must be cut near the edge connector. These traces may be identified in part by their width which is wider than that of the signal traces.

3. Address Decoding

The location of the various AD212 registers in the S-100 address space is determined by the five DIP switches SW1-SW5 on the mother board. (See AD212 Mother Board Switch Assignments.) These switches allow placement of the registers anywhere in the memory or I/O space of a conventional or extended memory system. Address comparison is done using four DM8136 ICs which are designated IC14, IC16, IC21 and IC31. These chips find a comparison on a given address line to be satisfied (true) when a high input from the S-100 bus has the corresponding DIP switch position OFF. The AD212 address space may be conceptually divided into three groups of eight lines each. The least significant group, A0 through A7, are always used no matter how the AD212 is configured. The middle group, A8 through A15, is active when memory-mapped addressing is selected on a computer system of conventional size or when I/O mapped addressing is selected on a newer system having sixteen bits of I/O addressing capability. The most significant lines, A16 through A23, are only used on extended memory systems where memory-mapped addressing is chosen.

To configure the AD212 in an eight bit I/O space, all address comparators are disabled except for IC31 by opening SW4-7 (position 7 of switch 4) and SW2-7.

Sixteen bit memory or I/O mapped operation is specified by closing SW4-7, opening SW2-7, and setting the left two switches of SW1 such that the lower side of the rockers are depressed. This simultaneously disconnects A16 and A17 from the bus while allowing A14 and A15 of IC16 and all inputs to IC21 to contribute to the comparison.

To operate the AD212 in a 24 bit extended memory-mapped system, the remaining eight most significant address lines must be enabled. This is done by closing SW4-7 and SW2-7 and by setting the left two switches of SW1 such that the upper side of the rockers are depressed.

The choice of memory or I/O-mapped operation is determined by the settings of SW5-5 and the right two switches of SW1. The IEEE S100 standard allows SMEMW to rise very late in a write cycle such that the AD212 may not have sufficient set up time for certain functions when used with fast processors if it is required to wait for the leading edge of SMEMW. Consequently, the preferred method of selection is to have SW1 permanently set to SOUT and SINP while SW5-5 is used to make the choice between memory or I/O. In this case, memory-mapped operation is selected when SW5-5 is on. This scheme eliminates a possible timing problem by eliminating the use of the SMEMW signal, but assumes that SINP and SOUT are stable during PDBIN and WR, respectively. For most processors (of if you didn't get the full gist of the above) set SW1 for SOUT and SINP (switches are down towared edge connector) and set SW5-5 ON for memory-mapped operation and SW5-5 OFF for I/O-mapped operation.

Unfortunately, the above technique will not work with some non-IEEE compatible processors such as Cromemco's Single Card Computer, where (incredibly) the status signals change at the same time as the timing signals PDBIN and WR. With such a processor, it is not possible to reliably use the false state of a status signal as our above selection technique does because circuit delays can cause skew between the timing and status signals thus producing momentary false selection when these signals change. With such processors, the proper method of selection is to leave SW5-5 open (off) and use SW1 to choose memory or I/O. This technique simply "ands" the status signals SINP and SOUT for I/O-mapped or SMEMR and SMEMW for memory-mapped with the results of the address comparison to form the signal BDSEL, which selects the AD212. I/O addressing is selected when the right two switches of SW1 have the lower part of their rockers depressed. Notice that neither of the above selection methods ever have SW5-5 on while SW1 is connected to SMEMW. This combination should rarely work properly due to the unique timing of SMEMW. The 74LS244 acts only as a receiver for these and other signals to minimize the load on the S100 bus.

When the four DM8136 ICs all find a true comparison, their open-collector outputs go high and they allow the signal BDSEL to become true. This signal enables five other chips, most important of which are the two 74LS138 address decoders, IC11 and IC12. These circuits decode address lines A1, A2 and A3 to produce eight possible read functions from IC12 and eight possible write functions from IC11. This is done by enabling IC11 with the WR signal and IC12 with the PDBIN signal. The address line A0 is not used in the decoding process because the AD212 is compatible with sixteen bit processors where A0 is undefined during sixteen bit transfers. This causes the AD212's functions to be addressable at pairs of address locations rather than at a single location as indicated in the description of the registers. Activation of various functions by the 74LS138's is straightforward in most cases where a register is loaded or read or a flip-flop cleared. The AM9513 timer chip has two read and two write addresses. Selection of these is accomplished by the 74LS08, IC8, which is connected in an "OR" configuration between the 74LS138 and the AM9513 and thus enables the timer chip for either of two addresses. Selection of one of these two addresses is determined by A1 which controls the C/D (control/data)input on the AM9513.

4. AM9513 Timer Circuit

The AM9513 is capable of performing either eight or sixteen bit transfers to the S100 bus. Considering eight bit transfers first, one finds that the chip does these using the bidirectional data lines DB0 through DB7. The most significant data lines must be held high during this time. This is done by using RP5 to pull them up while IC22 is disabled. To write to the timer I.C., the

bidirectional tranceiver, 74LS245, IC24 must be enabled by the occurence of WR and BDSEL. The direction of IC24 will be from the S100 bus to the timer as long as PDBIN is false. To read from the AM9513, a 74LS244, IC28, enables the timer data onto the S100 bus when the timer chip read select is true and S100 signal SXTRQ is false.

For sixteen bit data transfers, IC28 will never be enabled, but IC22 and IC24 will be active. For both reads and writes, IC24 behaves exactly as it did for eight bit transfers. The bidirectional tranceiver, 74LS245, IC22 is enabled whenever SXTRQ (sixteen request) is true and the AM9513 is selected for a read or a write operation. The timer chip read line is used to control the direction of IC22 so that it receives from the S100 bus during a write and drives the bus during a read. All sixteen bit transfers to the AD212 cause an acknowledgement signal, SIXTN, to be placed on the bus by IC4. This signal is true when SXTRQ and BDSEL are true. On power-up, the AM9513 assumes 8 bit operation and must be enabled for 16 bit operation by setting bit 13 of the Master Mode register as detailed in the AM9513 data sheet.

The AM9513 is potentially the slowest component of the AD212 and may not be fast enough to operate at full speed with fast processors. Consequently, IC7, IC9 and IC10 are used to create an optional wait state by lowering the ready line. Specifically, flip-flop IC10 is clocked true during PSYNC by the falling edge of the master timing signal, PHI, and false again on the next clock. Since PSYNC occurs for one clock period at the beginning of each bus cycle, IC10 generates a signal called "WAIT" which can be used to make the processor wait for one clock cycle. If SW3-5 is on, then IC9 will lower the RDY line when the AM9513 is addressed. This will occur when WAIT, A2, A3 and BDSEL are all true. In most cases this wait state will not be needed and SW3-5 can be left open.

The CS (chip select) input on the AM9513 is always enabled, but no action occurs unless the read or write lines are active also. A one megahertz, crystal controlled clock is fed to the timer chip by using a 74LS74, IC10, to divide the two megahertz clock from the S100 bus.

Each of the five counters in the AM9513 has three external connections associated with it. One is an output, one is a count source input, and one is a gated input. All of these are externally available after being buffered by two 74LS244's, IC17 and IC18, to a forty pin ribbon connector with interlaced grounds. In addition, a programmable divider signal called FOUT is accessible on pin 20. Five volt power is also available on this connector for powering a small amount of external logic. On the order of 100 milliamperes may be drawn from this source as long as enough air is provided to the regulator heatsink on the mother board to keep the regulator cool so that it doesn't shut down. These timer chip connections can provide several other special functions which will be described in the Interrupt and A/D sections.

5. The Data Acquisition Subsystem

The main component of the data acquisition subsystem is the large module on the daughter board which contains the 16 channel multiplexer, sample-and-hold, analog to digital converter and related control circuitry. The AD212 is currently designed to accept at least nine different modules from two manufacturers. These are the DT5701, DT5702, DT5703, DT5710, DT5712, DT5714, and DT5716 from Data Translation, Inc. and the MP6812 and MP6912A from Analogic Corp. These modules are not entirely plug compatible with one another so that a number of jumpers are required on the daughter board to compensate for the incompatibilities. There are also a number of optional modes of operation the selection of which requires additional jumper areas. The specific function of these jumpers will be described when the related part of the circuit is discussed.

5a. The Multiplexer

The A/D circuit can only convert one analog voltage to its digital equivalent at a time. Consequently, if it is desired to measure more than one voltage then some means of connecting different input signals to the A/D must be provided. This is done by the multiplexer which allows selection of any one of 16 input signals under program control. These input signals are designated channel 0 through channel 15 and connection to them is done on connector P1 on the daughter board.

There are two basic techniques for determining which channel is selected. The simpler of the two is to load the address of the desired channel into the module before each conversion. This is accomplished by setting bit 2 of the command register to a 1 and loading the address into the MUX (multiplexer) address register before the module is strobed. This holds the load enable input to the module low so that the internal counter is parallel loaded with the least significant four bits of the MUXADDR register IC25 when the module is strobed. This technique works well for random sampling of the channels or for repetitive sampling of a given channel. If repetitive scanning of more than one channel is desired, then the second basic technique is faster. Here the multiplexer automatically advances to the next sequential channel every time the module is strobed. This mode is enabled by setting bit 2 of the command register to a 0. The module, as it comes from the factory, would then continuously sequence through all 16 channels repetitively. The module outputs the address of the current channel as signals MXADOUT1, MXADOUT2, MXADOUT4, and MXADOUT8. These signals are connected to bits 0 through 3 of the status register, IC30, so that the program can always read the address of the current channel. The AD212 has additional circuitry consisting of IC1D, IC2D, RP1D, and SW1D. The lowest channel number desired is loaded into the MUX address register. As each strobe increments the channel number, IC1D compares the number in SW1D with the value on the MUXADOUT lines. When the module reaches the upper channel number, IC1D lowers the load enable input to the module so that the next strobe pulse loads the lower limit channel number from IC25 into the module rather than allowing the module to increment to the next channel. This act causes IC1D to raise the load enable input and the channel number incrementing resumes.

Probably the best use of this feature is to set SW1D equal to the number of channels is use assuming that channels are assigned contiguously from channel 0 upwards. Then the MUX address register can be used to select what subset of these channels are scanned. The most frequently scanned signals should be connected to the higher channel numbers.

The most significant four bits of the MUX address register and of SW1D are not used on the AD212 but rather are run to connector P3D. By adding expander boards, this provides for expansion for up to 256 input channels.

5b. Signal Input Options

The six pin jumper area "S" (See Jumper Area Numbering - Daughter Board) allows the multiplexer inputs to be configured as single-ended, differential, or psuedo-differential. The latter is a variation of the single-ended configuration where the common return line from the input signals is allowed to float with respect to the module's analog ground. By tying the return line to the low side of the differential input amplifier (pin 12B on the module) which is available on all modules but the DT5703, common mode noise voltages appearing between the return line and analog ground are rejected. Any single-ended module can be connected for psuedo-differential operation, but some of the modules come in only single-ended or only differential versions so that all three modes of operation may not be possible. A differential module may, of course, always be connected as a single-ended unit by grounding one of each differential input pairs, but this wastes half of the inputs in the process and gives no advantage over differential operation.

To connect a module for single-ended operation, jumper 1S to 2S. (See Jumper Area Numbering - Daughter Board) The multiplexer actually consists of two 8 channel units rather than one 16 channel one. This jumper connects the outputs of these two multiplexers together thus creating one 16 channel MUX. Next, jumper 3S to 4S thereby connecting the low input of the differential amplifier to the input signal return line. The high input of the differential amplifier is internally tied inside the module to MUX OUT HI which is jumper pin 1S. Finally, jumper 5S to 6S to connect the signal return line to analog ground. Psuedo-differential operation is achieved by leaving the last jumper off.

For true-differential operation, jumper 2S to 3S. This runs the multiplexed output of the low side of the differential input pairs to the low input of the differential amplifier. Thus, two eight channel multiplexers now work together to switch pairs of signal inputs into the high and low inputs of the differential amplifier. In general, this change also requires manipulation of the multiplexer address and control lines. Such changes depend strongly on the module type and may require attention to jumper area C. (See Jumper Area Number - Daughter Board) Differential operation should also have 5S jumpered to 6S.

The above description applies, at least in part, to all modules except for the DT5703 which is internally wired for differential operation and has no provision to make operational mode changes with external jumpers.

Notice that the signal input lines on P1D are not arranged in order of ascending channel number, but rather in order of ascending differential channel pairs. For example, channel 0 and channel 8 form the first pair, channel 1 and channel 9 form the second pair, and so on. this is to make it easier to have or to approximate the ideal of an input cable composed of twisted differential pairs. In reality, the common ribbon cable which would normally be used, has interlaced grounds which is optimum for single-ended operation but represents a compromise for differential operation.

MUX OUT HI and MUX OUT LO, which appear on module pins 11T and 11B are brought out to expansion connector P3D. If expansion modules are used in the system, their outputs are fed to the A/D through these lines. As a result, these lines must be shielded as well as the signal input lines.

5c. Gain, Range, and Polarity Options

All nine possible modules have the ability to perform conversions on input signals over the range 0 to 10 volts or ±10 to 10 volts, jumper selectable. Some modules also allow jumper selection of ranges 0 to 5 volts and -5 to 5 volts. In addition, most of the Data Translation modules allow selection of higher levels of gain eigher under software control or by adding resistor R2D depending upon which version of a given module model is ordered. Higher gains require waiting a longer time for the input amplifier to settle. Addition of capacitor C1D lengthens the time before the DLYOUT pulse occurs, which is usually used to determine the settling time allowed. Tables of values for R2D and C1D may be found in the module data sheets. Specific jumpering arrangements for jumper area A (analog) (See Jumper Area Numbering - Daughter Board) for the various modules may be found in the jumpering pages. Information on these pages may differ from that in the data sheets with regard to module pins 14T and 14B. These pins are identical inputs to the A/D converter and hence may be interchanged with no effect, thus accounting for two different descriptions in the documentation, both of which are correct.

For the MP6912 only, Analogic recommends that a filter capacitor be added to the +10 volt reference output having a value of 47 microfarads or greater at 20 volts. The MP6912 also allows having a jumper between 9A and 10A to change the input voltage range from a decimal scale to a binary scale. That is, a 10.00 volt range would become a 10.24 volt range and a 5.00 volt range would become a 5.12 volt range.

5d. Timing and Control Options

All module functions are initiated directly or indirectly by the rising edge of the STROBE pulse. The most straightforward method of operation has jumper 4C connected to either 5C or to 16C. In this case, the STROBE pulse causes the internal counter to receive or increment to a new multiplexer address. The multiplexer switches to a new channel and the signal to be converted propagates through the input circuitry to the A/D circuit. Since this process takes time, the conversion cannot begin on the rising edge of the STROBE pulse. Instead, STROBE starts a timer whose period is chosen to be just long enough for the input circuitry to stabely acquire the new channel. A negative going pulse called DLYOUT starts at the end of the timer interval. The above jumper routes DLYOUT to A/D TRIG- which starts the actual conversion. The signal EOC (End of Conversion) goes high at this time and remains high until conversion is complete and the digital data is stable on the module's output lines. EOC is used to immediately load the data into three 74LS374's, IC23, IC27 and IC29. The data is now available for reading by the CPU and the double buffering frees the module to begin another conversion cycle immediately. EOC also strobes two flip-flops called DONE and OVERRUN. DONE is left set by EOC if it was not already and is used to signal the CPU that the data is available. The act of reading the most significant data byte in IC29 also clears the DONE flop. Thus for eight bit transfers, if the software is arranged so that the most significant byte is read last, then the DONE flop will remain set until all of the data has been read. The OVERRUN flip-flop will always remain a zero as long as the DONE flop is cleared before the end of the next EOC pulse. More importantly, the OVERRUN flop will be set if new data is loaded into the 74LS374's before the CPU has read the previous data. This allows the user to operate at the highest possible coversion rates and still have confidence that he is not losing or perverting his data. Since checking the status of the OVERRUN flop after every data word is read could slow down the system, it is preferable to operate this flop in an interrupt mode so that the CPU is interrupted if and only if an overrun occurs.

The STROBE pulse may originate from one of several sources. The simplest means of generation is to write to port 4 which produces the signal ADSTRW, which serves as the strobe pulse. (See Register Assignments - Write) A gated external strobe input is provided on P3, pin 3, of the timer connector. This input is enabled when bit 3 of the command register is high. Notice that leaving bit 3 high without tying the external input low will prevent the use of ADSTRW. A conversion is initiated on the rising edge of the external strobe signal. If strobing at regular intervals is desired without requiring the attention of the CPU, the AM9513 can be a very flexible source of strobe pulses. The external strobe, pin 3, on P3 is conveniently located next to OUT5, pin 4 from the timer, thus allowing OUT5 to serve as the strobe source by simply sliding a

jumper onto this pair of pins. Another possible source of the STROBE pulses is through pin 12 of P3D. If this is used as an input to the A/D, then the jumper between 8C and 9C must be absent. This input is not gated and will always respond to a negative transition. P3D may be used in its normal role as the multiplexer expansion connector and still be available as an external strobe input due to the ability to daisychain ribbon cables. This same line also allows multiple AD212 systems to initiate conversions synchronously with one another. For this configuration, all P3D's, pin 12 must be tied together with a daisy-chained ribbon cable. All but one board must have jumper 8C to 9C absent, the remaining board providing the STROBE source.

The simplest way to obtain the maximum conversion rate of a module is to use jumper area F. This option is enabled by jumpering 3F to 4F, 4C to 16C, 5C to 17C, removing 19C to 20C and jumpering pins 2 and 3 (external strobe) together on P3 of the mother board. This causes the A/D module to free-run; strobing itself at its own maximum rate. This rate is the reciprocal of the sum of the conversion time and the DLYOUT signal and hence can be adjusted to some extent on certain modules by the knowledgable user by adjusting the DLYOUT signal. Bit 3 in the command register now serves as a run/stop control such that a zero causes continuous conversions. It is not necessary to send out a strobe in software using the free-run mode. See page 56 for further programming clarification.

The free run mode of operation will also function in an overlapped (pipeline) manner by jumpering 1F to 2F instead of 3F to 4F. In addition to all of the restrictions applying to overlapped operation described below, an idiosyncracy internal to the A/D module prevents it from loading or incrementing to a new channel while in the overlapped, free-run mode. The desired channel must be loaded while the A/D module is stopped.

The free-run feature is not available with the MP6812 or the DT5703.

One way to increase the module's throughput is to advance to a new input channel and allow it to start settling before the current conversion is complete. This is known as overlapped or pipelined operation. This mode of operation is enabled by jumpering AD TRIG- which is 5C or 16C depending on the module to 17C which is the STROBE pulse. This causes the STROBE pulse to simultaneously initiate (rather than sequentially initiate) an A/D conversion and the advance to the next channel. This complicates the acquisition process because two strobe pulses are normally required to make a measurement. The first STROBE pulse causes the multiplexer to point to the desired channel; the second one starts the A/D conversion for the channel that the first pulse caused the MUX to point to. The second pulse also simultaneously advances the MUX to the next desired channel. One must take care when writing the software that a given data word is associated with the correct channel number when using overlapped operation. Highest throughput is obtained when the strobe period is slightly longer than either the input amplifier settling time or the A/D conversion time, whichever is greater. This mode of operation can be especially fast if only one channel is being measured because now one need not wait for the input amplifier to settle due to channel switching. The throughput is now limited only by the A/D conversion time if the input signal is not above the bandwidth of the input amplifier. The latter could occur with high gain modules. Single channel, high gain measurements in this mode may provide an order of magnitude or more increase in throughput.

Overlapped operation is not recommended when the amplifier settling time is short. Taking the MP6912A as an example, the mux switching time and the amplifier settling time combined are 1 microsecond while the sample-and-hold circuit requires 4 microseconds to complete a sampling. Since the sample-and-hold cannot simultaneously sample one voltage while holding another, the 4 microsecond sample time must be added to the MP6912A's 5 microsecond conversion time. Thus, overlapped operation saves only 1 microsecond by reducing the total cycle time to 9 microseconds. For the MP6912A overlapped operation requires readjusting the DLYOUT time from its normal 5 microseconds to 9 microseconds to give the sample-and-hold circuit 4 microseconds to do a sample. This marginal improvement in speed can cause seriouts problems if the MUX samples channels with widely varying voltages. Since the sample-and-hold is not a perfect device, a rapidly changing signal on its input may feed thru slightly and cause drastic changes in the resulting value of the A/D conversion which is going on simultaneously.

Another way to increase throughput is to have the CPU wait for the completion of conversions. This feature is enabled by closing SW3-6 which allows IC4 pin 6 to lower the CPU's PRDY line. This causes the CPU to enter a wait state for as long as the PRDY line is low. Also, bit 7 of the command register must be a one giving the programmer software control of this feature. Bit 7 performs a double function on the AD212 since it also is used to enable an interrupt when the DONE flop is set. Because of this, interrupts caused by the DONE flop must be disabled. For vectored interrupts this is easily achieved by not connecting the DONE pin on the vectored interrupt header. If polled interrupts from some of the remaining interrupt sources are desired at the same time, the wait feature is enabled, then the trace from IC4 pin 3 must be cut. Programming is arranged such that all necessary setup operations are performed first, followed by software generation of the A/D strobe pulse if that is the strobe source used. Finally, for sixteen bit transfers, a read instruction to port 4 is executed. This causes the signal ADR to propagate through IC13 and IC15 to make IC4 pin 4 true (high). If bit 7 of the command register IC26 is high, then IC5 pin 10 will be true and assuming that the conversion is not yet complete, IC3 will cause IC5 pin 9 to be true thus making the ready line low. The CPU will now wait until the DONE flop is set making the ready line high again. The CPU will continue where it left off by immediately finishing the instruction to read the new number in the data register thus saving the time that would otherwise be required to test the DONE bit in the status register for completion of a conversion. The situation for eight bit transfers is very similar except that the wait occurs when the CPU reads the lower eight data bits from port 2. When the wait is over, the CPU then reads the high eight data bits from port 4.

The WAIT Function

The proposed IEEE S100 standard allows ridiculously little setup time on the PRDY line which might make the AD212 harder to use with processors which follow this standard too closely. Closing SW3-8 helps solve this problem by pulling the ready line down sooner. Unfortunately, a compromise is involved because the ready line is pulled down for one clock cycle during PSYNC at the beginning of every instruction whether IC4 wants the CPU to wait or not. This, of course, slows down the CPU. The only alternative to this solution involves adding several additional integrated circuits which would probably not be justified for most users.

6. The Status Register

An eight bit status register is available for interogation by the CPU at any time. (See Register Assignments - READ) The four bits of the channel counter in the A/D module form the lower bits of the status register. OVERRUN and DONE flip-flops may be read in bits 6 and 7, respectively. Timer interrupt flip-flops 1 and 2 may be read in bits 4 and 5. The timer flip-flops are described in the interrupt section.

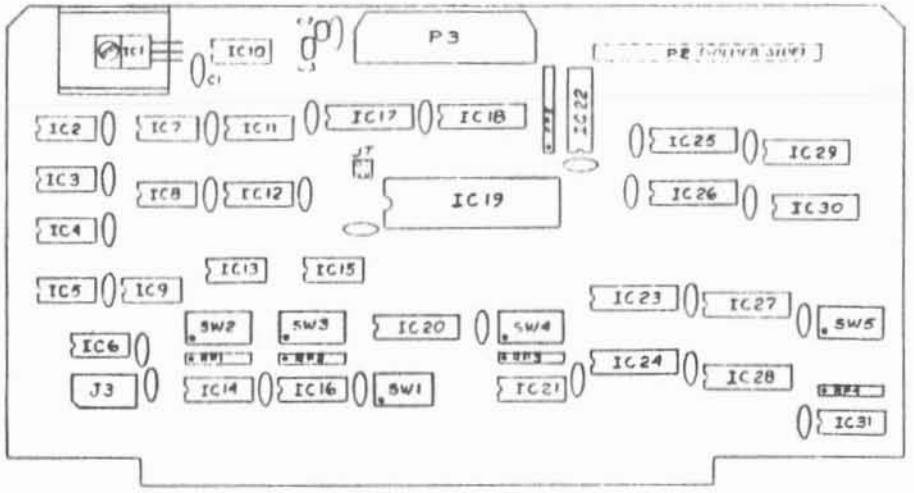
7. Interrupts

The AD212 can provide either polled or vectored interrupts from any combination of four sources. These sources are OVERRUN, DONE, and timer interrupts 1 and 2. The ability of a given source to generate an interrupt may be enabled or disabled by setting or clearing, respectively, the corresponding bit in the command register. For polled interrupts, the state of each source may be examined by the CPU in the upper four bits of the status register. Vectored interrupts are enabled by soldering wires from the desired source pins to the desired vector priority level pins VI0 through VI7 on the vectored interrupt header. Any combination of connections is allowed here; ie., each source may go to a different vector priority level, or at the other extreme, all sources may be connected to the same priority level pin. Polled and vectored operation should not be simultaneously enabled.

Operation with vectored interrupts is preferred over polled operation because the software overhead associated with identifying the source of a polled interrupt can slow down a system significantly. Unfortunately, vectored interrupts usually require additional hardware in an S100 machine.

Note that timer interrupts 1 and 2 do <u>not</u> refer to AMD 9513 timers 1 and 2. Rather, interrupt 1 is generated (when enabled) by AMD 9513 timer 5. Interrupt 2 is generated, when enabled, either by AMD 9513 timer 2 or 3 depending on how jumpers 1T, 2T, and 3T are set. If 1T and 2T are jumpered together, timer 3 is gated to the interrupt 2 line and if 1T and 3T are jumpered together timer 2 is gated to the interrupt 2 line.

REV	ZONE	ENG NO	REVISION	DRN	CKD	DATE



ALL CAPS ARE .1 uF EXCEPT WHERE NOTED

ITEM	PART NO	QTY	DESCRIPTION	DESIGNATION
1		1	280#	IC1
2		1	HEAT SINK & INS. #	
3		3	74LS74	IC2,3,17
4		1	7403	IC4
5		2	74LS00	IC5,15
6		1	7407	IC6
7		1	74LS14	IC7
8		1	74LS08	IC8
9		1	7482	IC9
10		2	74LS138	IC11,12
11		1	74LS32	IC13
12		4	DM8136	IC14,16,21,31
13		5	74LS244	IC17,18,20,28,30
14		1	AM9513	IC19
15		2	74LS245	IC24,22
16		2	74LS273	IC25,26
17		3	74LS374	IC29,23,27
18		5	2.7K RES NET	RP1,2,3,4,5
19		1	330pF CAPACITOR	C1
20		2	22uF "	C2,C3
21		26	.1uF "	
22		1	2x2 MALE HDR	J1
23		4	206-8 SWITCH	SW-2,3,4,5
24		1	7LC04 SWITCH	SW-1
25		1	DIP HEADER	J3
26		1	8x80 90° CONNECTOR	P3
27		1	8x35 MALE CONNECTOR	P2
28				

ASSY.	R/M	ITEM	PART NO	REQ	DESCRIPTION
MATERIAL			DO NOT SCALE DRAWING		TECMAR INC CLEVE OHIO
FINISH			TITLE COMP LAYOUT AD212 MOTHER BD		
DRN. DATE	CKD. DATE	APP. DATE	SCALE	MOD NO REV B	C

S100 P1

RP1 +5V

DM 8136 IC14 — A23 A22 A21 A20 A19 A18 — STR OUT

SW-2

RP4 +5V

SW-2

S100 P1 VECTORED INTERRUPT JUMPER HEADER — VI7 VI6 VI5 VI4 VI3 VI2 VI1 VI0

IC6 07 IC6 07 IC6 07

7403 IC4 — 7422 IC9 — LS00 IC5 — LS00 IC5 — LS00 IC5 — 7403 IC4

+5V

INT PSYNC Φ — SW3

LS14 IC7 WAIT

LS74 IC10

RP2 +5V

SW1 SW3

DM 8136 IC16 — A15 A14

33 THRU 42 P2

RP3 +5V SW4

DM 8136 IC21 — A13 A12 A11 A10 A9 A8

SW4

RP4 +5V SW-5

DM 8136 IC31 — A7 A6 A5 A4

2 MHZ CLOCK

+10V +20V −20V P2 29 30

Z7 Z8 22 µf IC2 .1µf 7805 IC1 +5V 22 µf C3

LS 244 IC 20 — A3 A2 A1 BOC SXTRQ WR SOUT SMEMW SINP SMEMR PDBIN — SW1

LS32 IC13 IC7 LS00 IC15 LS00

LS 245 IC24 — DO7 DO6 DO5 DO4 DO3 DO2 DO1 DO0

PRDY SIXTN — SW3

7422 IC9 7403 IC4

LS08 IC8 — LS 138 IC11 — OVRNCL INTCLZ INTCL1 ADSTRW MUXADRW EMDW

BDSEL

LS08 IC8 — LS 138 IC12 — ADR LABR STATR

LS32 IC13 LS08 IC8

IC13 LS32 IC7 LS 14

DI

LS 245 IC22 — DI7 DI6 DI5 DI4 DI3 DI2 DI1 DI0

LS 244 IC28

DO

RP5 +5V

C/D CS

AM 9513 IC 19

DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

X2 X1

+5V

LS 74 IC10 — TIMER INT 1 — TIMER INT 2

LS 273 IC26 CMD — LS 273 IC25 MUX ADDR

MUX ADDR OUT 128 MUX ADDR OUT 64 MUX ADDR OUT 32 MUX ADDR OUT 16 MUX ADDR IN 8 MUX ADDR IN 4 MUX ADDR IN 2 MUX ADDR IN 1 GSO GS1 LOAD EN

LS 244 IC30 STATUS — MUX ADDR OUT 8 MUX ADDR OUT 4 MUX ADDR OUT 2 MUX ADDR OUT 1

STROBE

LS 74 IC3 — DONE — OVER RUN

EOC

330 Pf

P3 DONE EXT. STROBE

LS 374 IC29 — BIT 15 BIT 14 BIT 13 BIT 12 BIT 11 BIT 10 BIT 9 BIT 8

LS 374 IC 27 — BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0

LS 244 IC17 — GT1 GT2 GT3 OUT 5 OUT 4 OUT 3 OUT 2 OUT 1 — 2T 1T 3T

LS 244 IC18 — GT5 GT4 SRC5 SRC4 SRC3 SRC2 SRC1 FOUT — THRU

P2

NOTE: ALL RESISTORS ARE 2.7 K Ω

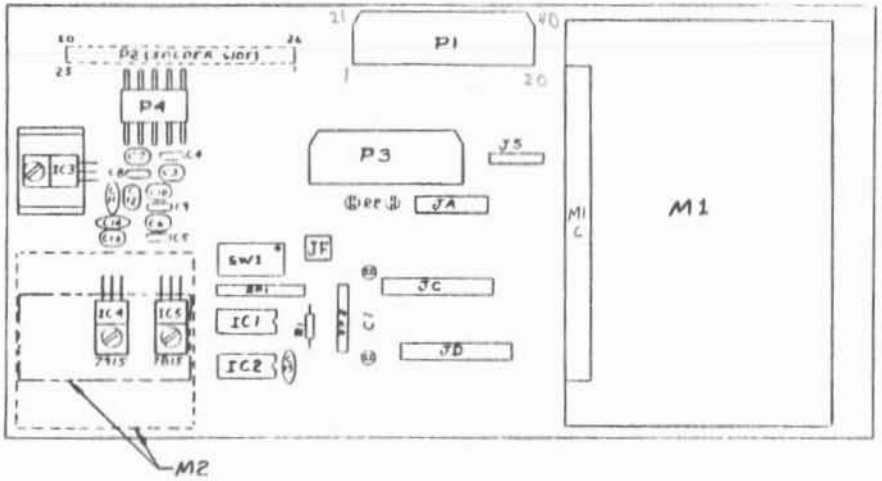
UNUSED GATES	REFERENCE DESIGNATIONS LAST USED	NOT USED

TECMAR INC

TITLE SCHEMATIC AD 212 MOTHER BOARD

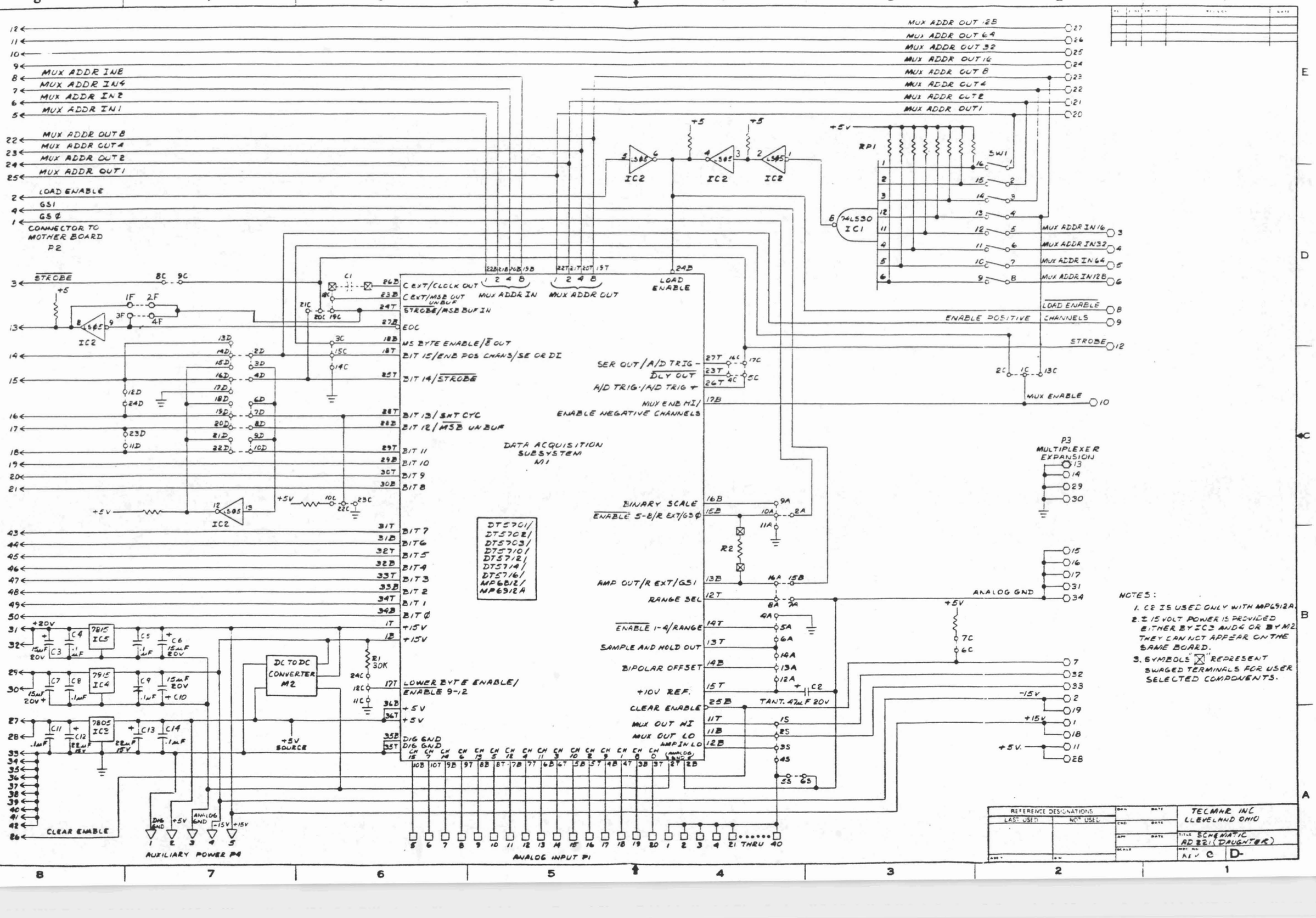
REV C D

REV.	ZONE	ERO NO	REVISION	DRN	CKD	DATE



ITEM	PART NO	QTY	DESCRIPTION	DESIGNATION
1		1	MP6812 (TYP)	M1
2		1	AUTOBUS BUS CONVERTER	M2
3		1	UA7805	IC3
4		1	MC7818	IC5
5		1	DM74LS05	IC1
6		1	SN74LS30	IC2
7		1	30K ¼W 5%	R1
8		1	USER SELECTED	R2
9		2	8.2K RES. NET	RP1, 2
10		1	2pb-K SWITCH	SW1
11		1	HEAT SINK 8107-M	
12		1	4 PIN SIDE MALE HDR.	J5
13		1	3 PIN SIDE MALE HDR.	JA
14		2	15 PIN MALE HDR.	JC, JD
15		1	25 PIN MALE HDR.	P2
16		1	5 PIN BOARDMOUNT SOCKET	P4
17		1	2x20 MALE CONN.	P1
18		1	2x17 MALE CONN.	P3
19		3	FORKED STANDOFF	
20		3	1µF CAPACITOR	C11, C14, C15
21		4	.1µF CAPACITOR	C4, C5, C8, C9
22		4	15µF CAPACITOR	C3, C6, C7, C10
23		2	22µF CAPACITOR	C12, C13
24		1	USER SELECTED	C1
25		1	MICROPHONE ELEMENT	MIC
26		1	MC7915	IC4

ASSY.	B/M	ITEM	PART NO.	REQ	DESCRIPTION
MATERIAL			DO NOT SCALE DRAWING		TECMAR INC CLEVE. OHIO
FINISH					
DRN. DATE	CKD. DATE	APP. DATE	TITLE COMP LAYOUT AD221 DAUT. BD.		
			SCALE	MOD NO REV. C	C


MUX ADDR IN8
MUX ADDR IN4
MUX ADDR IN2
MUX ADDR IN1
MUX ADDR OUT8
MUX ADDR OUT4
MUX ADDR OUT2
MUX ADDR OUT1
LOAD ENABLE
GS1
GSØ
CONNECTOR TO MOTHER BOARD P2
MUX ADDR OUT128
MUX ADDR OUT64
MUX ADDR OUT32
MUX ADDR OUT16
MUX ADDR OUT8
MUX ADDR OUT4
MUX ADDR OUT2
MUX ADDR OUT1
+5V
RP1
SW1
74LS30 IC1
MUX ADDR IN16
MUX ADDR IN32
MUX ADDR IN64
MUX ADDR IN128
LOAD ENABLE
ENABLE POSITIVE CHANNELS
STROBE
MUX ENABLE
IC2
74LS05
STROBE
C EXT/CLOCK OUT
C EXT/MSB OUT UNBUF
STROBE/MSB BUF IN
EOC
MS BYTE ENABLE/Ē OUT
BIT 15/ENB POS CHANS/SE OR DI
BIT 14/STROBE
BIT 13/SMT CYC
BIT 12/MSB UNBUF
BIT 11
BIT 10
BIT 9
BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT Ø
+15V
+15V
LOWER BYTE ENABLE/ ENABLE 9-12
+5V
+5V
DIG GND
DIG GND
MUX ADDR IN
MUX ADDR OUT
LOAD ENABLE
SER OUT/A/D TRIG-
DLY OUT
A/D TRIG·/A/D TRIG +
MUX ENB HI/ ENABLE NEGATIVE CHANNELS
DATA ACQUISITION SUBSYSTEM M1
DT5701/ DT5702/ DT5703/ DT5710/ DT5712/ DT5714/ DT5716/ MP6812/ MP6912A
BINARY SCALE
ENABLE 5-8/R EXT/GSØ
AMP OUT/R EXT/GS1
RANGE SEL
ENABLE 1-4/RANGE
SAMPLE AND HOLD OUT
BIPOLAR OFFSET
+10V REF.
CLEAR ENABLE
MUX OUT HI
MUX OUT LO
AMP IN LO
R1 30K
R2
C2 TANT. 47µF 20V
ANALOG GND
+5V
-15V
+15V
+5V.
P3 MULTIPLEXER EXPANSION
DC TO DC CONVERTER M2
+5V SOURCE
C1
C3 15µF 20V
C4 .1µF
C5 .1µF
C6 15µF 20V
C7 15µF 20V
C8 .1µF
C9 .1µF
C10 15µF 20V
C11 .1µF
C12 22µF 15V
C13 22µF 15V
C14 .1µF
7815 IC5
7915 IC4
7805 IC3
CLEAR ENABLE
DIG GND
+5V
ANALOG GND
-15V
+15V
AUXILIARY POWER P4
ANALOG INPUT P1
21 THRU 40
NOTES:
1. C2 IS USED ONLY WITH MP6912A.
2. ± 15 VOLT POWER IS PROVIDED EITHER BY IC3 AND/OR BY M2. THEY CANNOT APPEAR ON THE SAME BOARD.
3. SYMBOLS "⊠" REPRESENT SWAGED TERMINALS FOR USER SELECTED COMPONENTS.
REFERENCE DESIGNATIONS
LAST USED
NOT USED
TECMAR INC
CLEVELAND OHIO
TITLE SCHEMATIC AD 221 (DAUGHTER)
REV C
D-

SWITCH AND JUMPER SUMMARY

The following two figures provide a summary of the switch functions and settings on the mother and daughter boards. The tables below also provide this information.

Function of Switches - Organized by Switch Number

Switch * Number	Position On[1]	Position Off[2,3]	Fuction
Mother Board			
1-1, 1-2	X		Enables 24 bit addressing
1-3, 1-4	X		Selects SMEMR and SMEMW
		X	Selects SOUT and SINP
2-1	X		Disables address line A23
2-2	X		Disables address line A22
2-3	X		Disables address line A21
2-4	X		Disables address line A20
2-5	X		Disables address line A19
2-6	X		Disables address line A18
2-7	X		Enables 24 bit addressing
		X	Disables 24 bit addressing (enable 16 bit memory or I/O mapped operation)
3-1	X		Disables address line A17
3-2	X		Disables address line A16
3-3	X		Disables address line A15

* First number refers to switch number; second number refers to switch position.

1 If upper portion of switch is depressed = ON

2 If lower portion of switch is depressed = OFF

3 The function in the OFF position will only be described if it is something other than the opposite of the ON position function.

Switch Number	Position On	Position Off	Function
3-4	X		Disables address line A14
3-5	X safety		Generates 1 wait state (may rarely be needed by AM 9513)
		X	Disables wait state generator
3-6	X for ADR5!		Enables CPU halt until end of conversion
3-7	X	MAKES BIG difference!	Enables polled interrupts
3-8	X needed!		If CPU wait for conversion switch is on (SW 3-6), then this may need to be on if CPU is too fast
		X	If CPU wait for conversion switch is on (SW 3-6) and CPU is not too fast
4-1	X		Disables address line A13
4-2	X		Disables address line A12
4-3	X		Disables address line A11
4-4	X		Disables address line A10
4-5	X		Disables address line A9
4-6	X		Disables address line A8
4-7	X		Enables 16 bit or 24 bit addressing
5-1	X		Disables address line A7 (DISABLE) = compare A7 against 0 when on
5-2	X		Disables address line A6
5-3	X		Disables address line A5
5-4	X		Disables address line A4
5-5	X		I/O or memory mapped [4]
		X	I/O or memory mapped (see SW1-3,4)

[4] See insert on AD212 Mother Board Switch Assignments and discussion in AD212 Circuit Description and SET-UP Guide.

Switch Number	Position On	Position Off	Function
Daughter Board			
1D-2	X		Add 1 channel to maximum channel reached during auto-incrementing
1D-3	X		Add 2 channels to ...
1D-3	X		Add 4 channels to ...
1D-4	X		Add 8 channels to ...
1D-5	X		Add 16 channels to ...
1D-6	X		Add 32 channels to ...
1D-7	X		Add 64 channels to ...
1D-8	X		Add 128 channels to ...

SWITCHES ORGANIZED BY FUNCTION

Mother Board

8 bit I/O space (conventional 8 bit systems - I/O mapped)

SW4-7	OFF
SW2-7	OFF

16 bit memory or I/O space (conventional 8 bit systems - memory mapped or extended addressing systems - I/O mapped)

SW4-7	ON
SW2-7	OFF
SW1-1, 1-2	lower side depressed

24 bit extended addressing systems - memory mapped

SW4-7	ON
SW2-7	ON
SW1-1, 1-2	upper side depressed

All systems - memory mapped (typical)

SW5-5	ON
SW1-3, 1-4	lower side depressed

All systems - I/O mapped (typical)

SW5-5	OFF
SW1-3, 1-4	lower side depressed

Memory mapped (non IEEE S100, i.e. Cromemco Single Card Computer)

SW5-5	OFF
SW1-3, 1-4	upper port depressed

I/O mapped (non IEEE S100, i.e. Cromemco Single Card Computer)

SW5-5	OFF
SW1-3, 1-4	lower port depressed

Generates one wait state for user with timer and fast CPU (usually leave SW3-5 OFF).

SW3-5	ON to generate wait state for AM 9513

To have CPU wait for completion of conversion:

1) Set SW3-6 to ON

2) Set bit 7 of command register (write register 0 or 1)

3) Disable interrupts caused by DONE by not connecting the DONE pin on the vectored interrupt header or cutting the trace from IC4 pin 3.

4) Set SW3-8 to ON only for fast CPU's (usually leave OFF)

Daughter Board

To set the maximum channel for auto incrementing: Set the switches to ON that add up to the maximum channel desired using auto incrementing.

	Number of channels to add
SW1D-1	1
SW1D-2	2
SW1D-3	4
SW1D-4	8
SW1D-5	16
SW1D-6	32
SW1D-7	64
SW1D-8	128

For example, if channel 11 is the last channel to be converted before returning to the initial channel, then SW1D-1, 2 and 4 should be turned on.

JUMPERS

Mother Board

Enable interrupts from AM 9513 OUT2 line

1T to 3T

Enable interrupts from AM9513 OUT3 line

1T to 2T

To count number of A/D conversions:

P3, pin 16 (DONE) to P3, pin 15 (SRC 4)

OR

P3, pin 16 (DONE) to P3, pin 17 (SRC 3)

Daughter Board

Area C on the daughter board may also need to be changed --

Signal/Input Options -- See Jumpering diagrams

Single-ended operation

1S to 2S
3S to 4S
5S to 6S

Psuedo-differential operation

1S to 2S
3S to 4S

True-differential operation

2S to 3S
5S to 6S

Gain, Range, Polarity -- See specific jumpering arrangements on jumpering pages.

INTERRUPTS

Polled interrupt enabled

SW3-7 ON

Vectored interrupts

Enabled by soldering wire from desired source (OVERRUN, DONE, Timer interrupts 1 and 2) to desired vector priority level pins VI0 thru VI7 -- See AD212 Mother Board Switch Assignments.

TIMING AND CONTROL OPTIONS

Normal operation of STROBE

4C to 5C or 16C (module dependent)

-- See Jumper diagrams

Overlapped or Pipelined Operation (advance to a new input channel and allow it to start settling before the current conversion is complete).

17C to 5C or 16C (module dependent)

-- See Jumpering diagrams

Possible sources for STROBE (start conversion) pulse:

1) Write to Port 4

2) P3 pin 3 - gated external strobe
   enabled when bit 3 of command register (WRITE register 0 or 1) conversion is set
   initiated on rising edge of external strobe signal

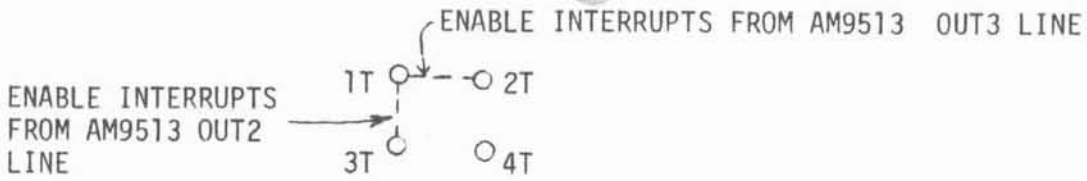
3) Strobing at regular intervals using OUT 5 of AM 9513 timer
   I.C. pin 3 on P3 (external strober) connected to pin 4 on P3 (OUT 5 of AM 9513)

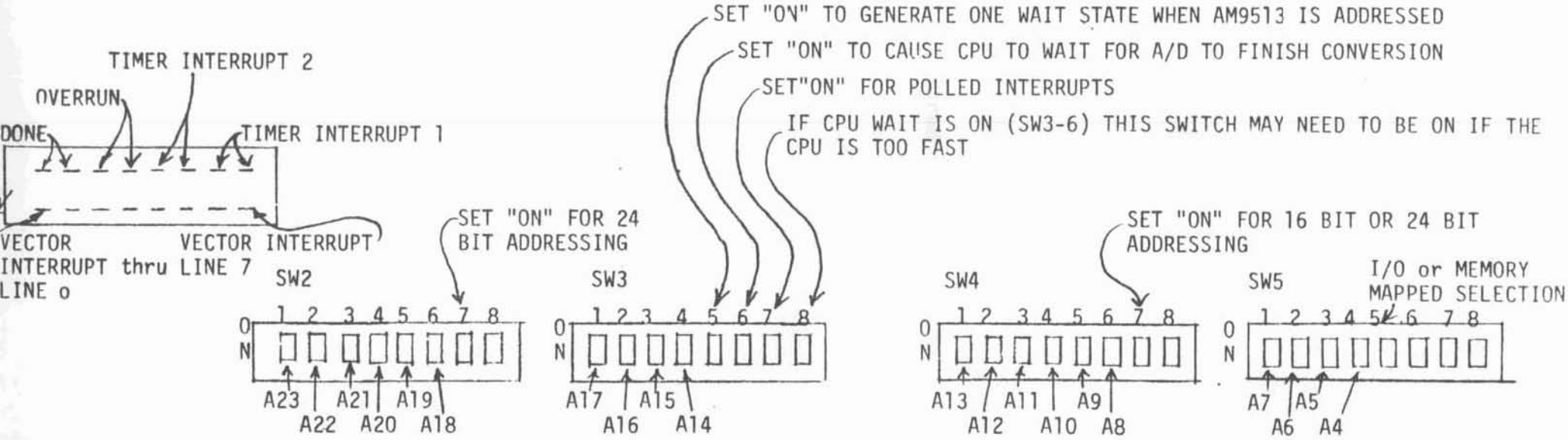
4) P3D pin 12 - not gated external strobe
   remove jumper from 8C to 9C
   conversion is initiated by a negative transition

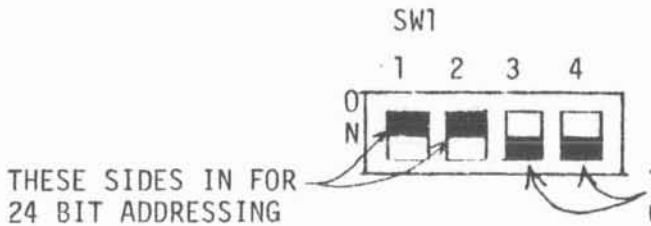
CONVENTIONS FOR JUMPERS

SOLID LINE ——— NECESSARY JUMPER BUT NOT USER SELECTABLE OPTION (FACTORY SET)

DASHED LINE - - OPTIONAL JUMPER FOR USER SELECTABLE OPTION

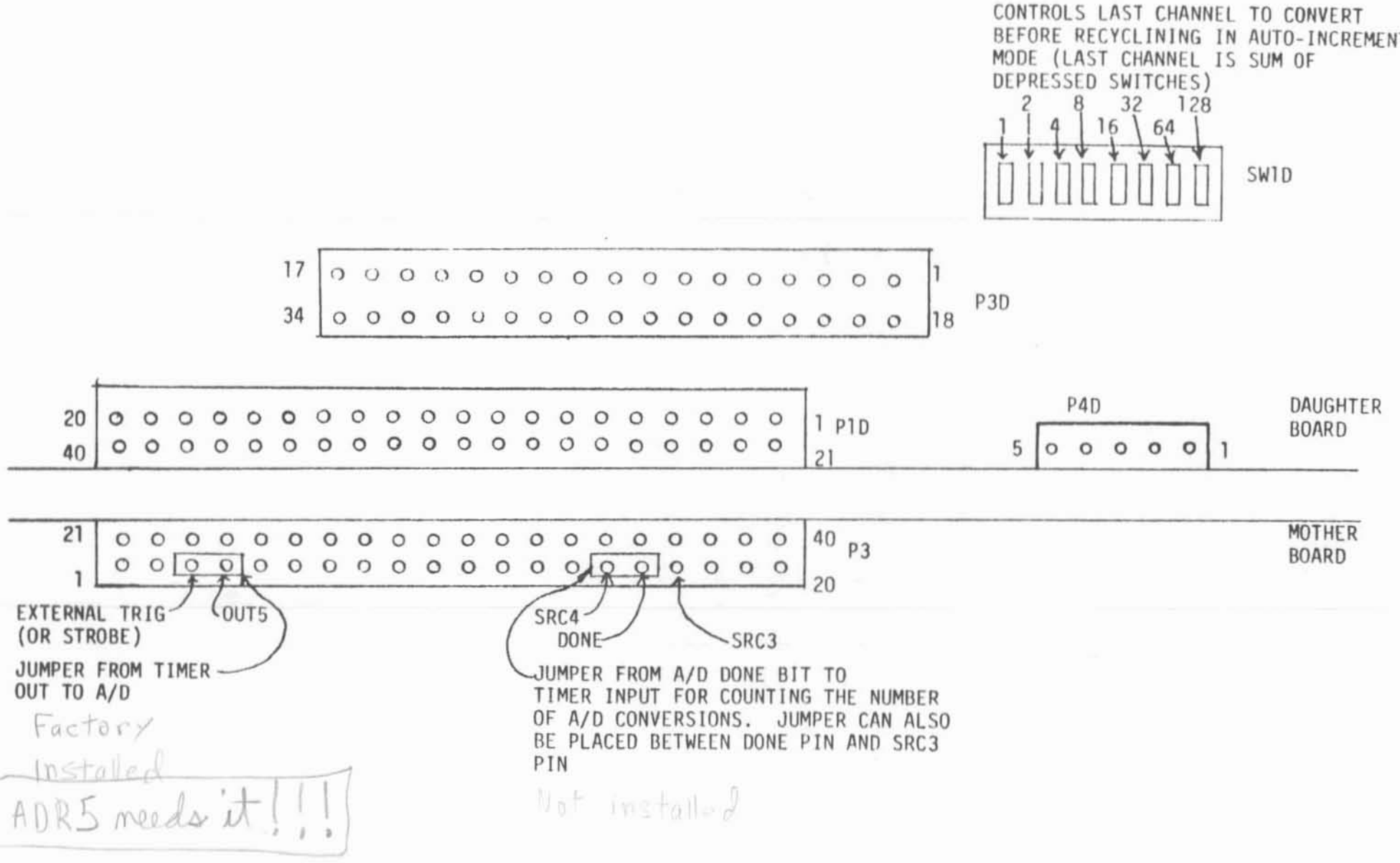



SET "ON" TO GENERATE ONE WAIT STATE WHEN AM9513 IS ADDRESSED
SET "ON" TO CAUSE CPU TO WAIT FOR A/D TO FINISH CONVERSION
SET"ON" FOR POLLED INTERRUPTS
IF CPU WAIT IS ON (SW3-6) THIS SWITCH MAY NEED TO BE ON IF THE CPU IS TOO FAST
TIMER INTERRUPT 2
OVERRUN
DONE
TIMER INTERRUPT 1
VECTOR INTERRUPT thru LINE 0
VECTOR INTERRUPT LINE 7
SET "ON" FOR 24 BIT ADDRESSING
SET "ON" FOR 16 BIT OR 24 BIT ADDRESSING
I/O or MEMORY MAPPED SELECTION
SW2
SW3
SW4
SW5
ON
1 2 3 4 5 6 7 8
A23 A22 A21 A20 A19 A18
A17 A16 A15 A14
A13 A12 A11 A10 A9 A8
A7 A6 A5 A4


SW1
1 2 3 4
ON
THESE SIDES IN FOR 24 BIT ADDRESSING
THESE SIDES IN TO SELECT SOUT AND SINP
OTHER SIDES IN TO SELECT SMEMR AND SMEMW

		SW5-5 ON	SW5-5 OFF
SW1-3,4	SINP + SOUT	MEMORY MAPPED	I/O MAPPED
	SMEMR + SMEMW	DO NOT USE	MEMORY MAPPED

AD212 MOTHER BOARD SWITCH ASSIGNMENTS



OUTPUT CONNECTORS FOR AD212

P3(TIMER, STROBE, DONE)-CONNECTOR PINOUTS

PIN NUMBER	FUNCTION
21-40	GROUND
16	DONE
3	EXTERNAL STROBE
4	OUT 5
9	GT 5
14	SRC 5
5	OUT 4
10	GT 4
15	SRC 4
6	OUT 3
11	GT 3
17	SRC 3
7	OUT 2
12	GT 2
18	SRC 2
8	OUT 1
13	GT 1
19	SRC 1
20	FOUT
1, 2	+ 5 VOLTS

P4D-CONNECTOR PINOUTS

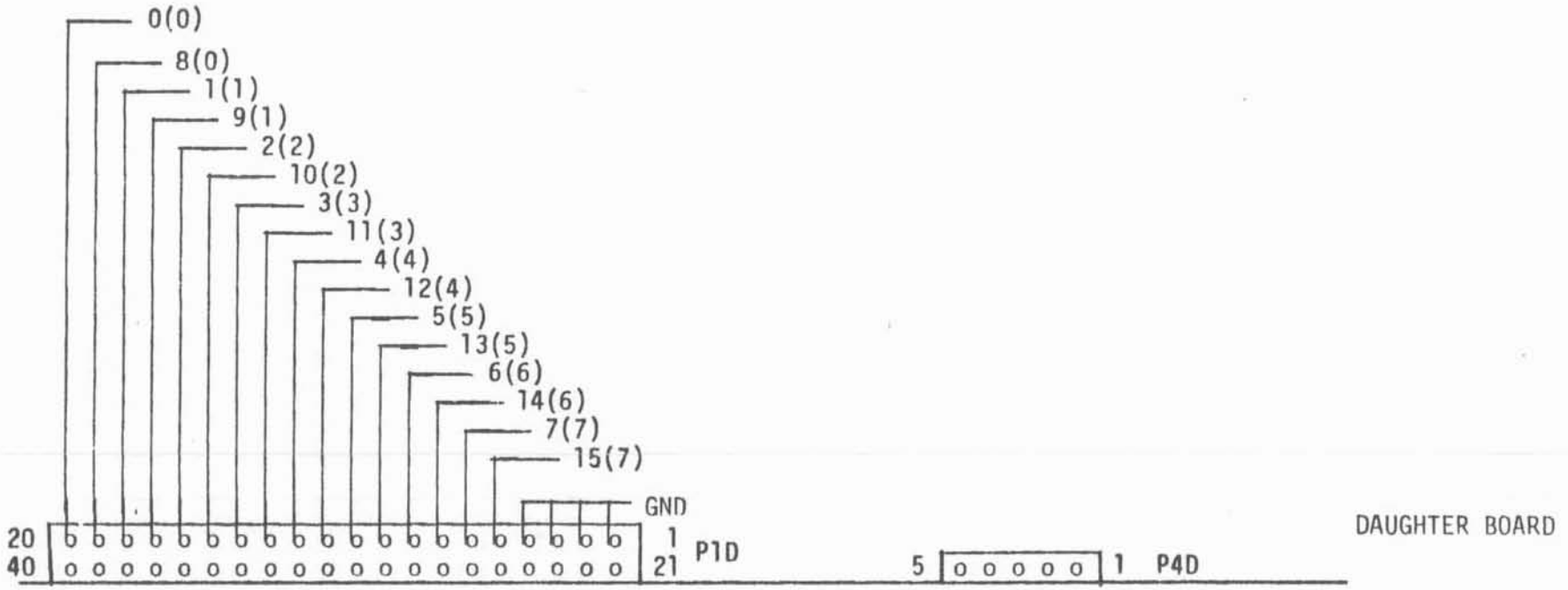
PIN NUMBER	FUNCTION
5	+15 VOLTS
2	+ 5 VOLTS
1	GROUND-DIGITAL
4	-15 VOLTS
3	GROUND-ANALOG

P1D-CONNECTOR PINOUTS

Pin Number	Function		
1,2,3,4 21-40	ANALOG GROUND		
20	SE INPUT CHANNEL 0	DI INPUT CHANNEL	0
19	8		0
18	1		1
17	9		1
16	2		2
15	10		2
14	3		3
13	11		3
12	4		4
11	12		4
10	5		5
9	13		5
8	6		6
7	14		6
6	7		7
5	15		7

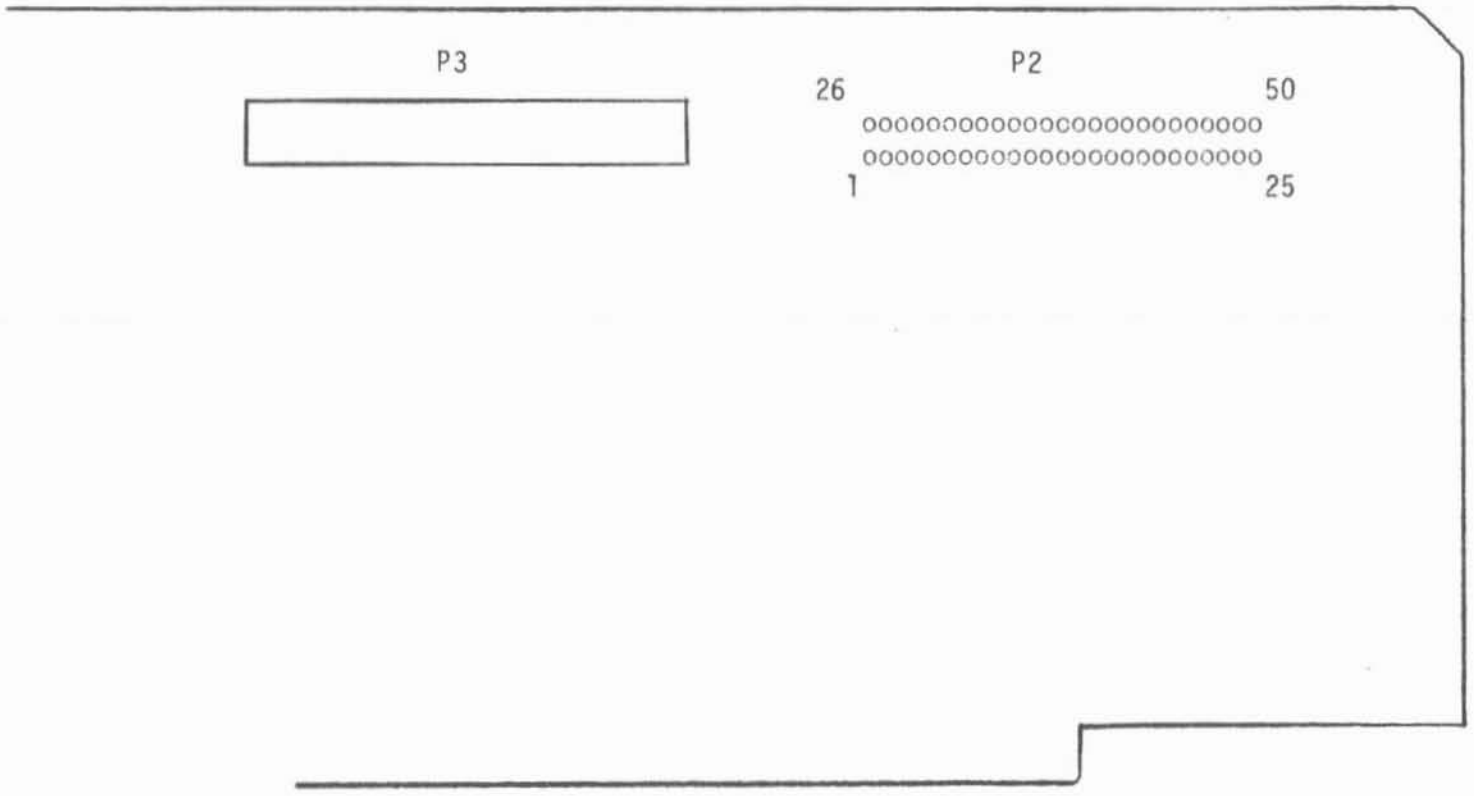
For use with Data Translation modules in the Differential Input (DI) configuration where there is no impedance between one of the inputs and analog ground, it is necessary to connect a resistor ($\simeq$ 100 KΩ) between that input and analog ground.

Be sure and terminate all unused inputs (connect unused input to ground).



INPUT SIGNAL CONNECTORS FOR SINGLE ENDED INPUTS AND (DIFFERENTIAL INPUTS)

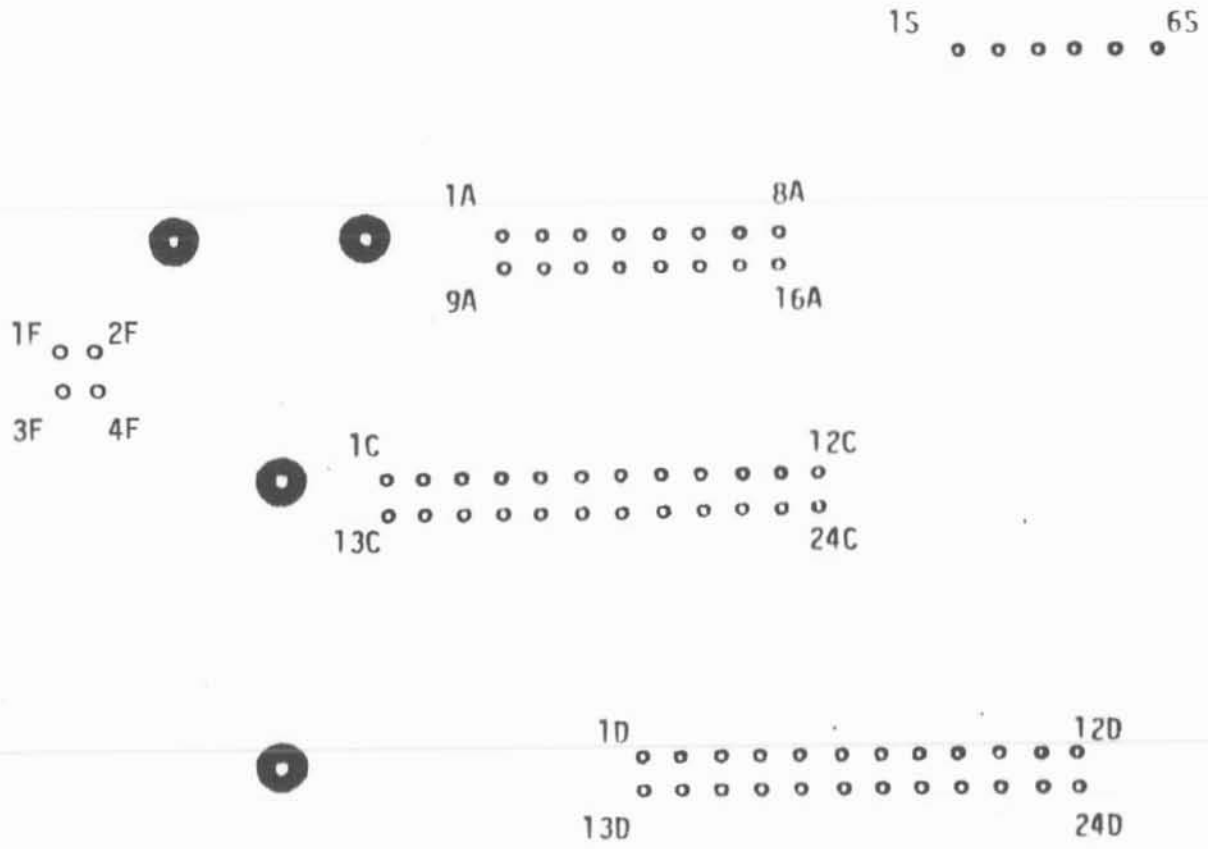
from component side - orient P1 & P4 as in drawing



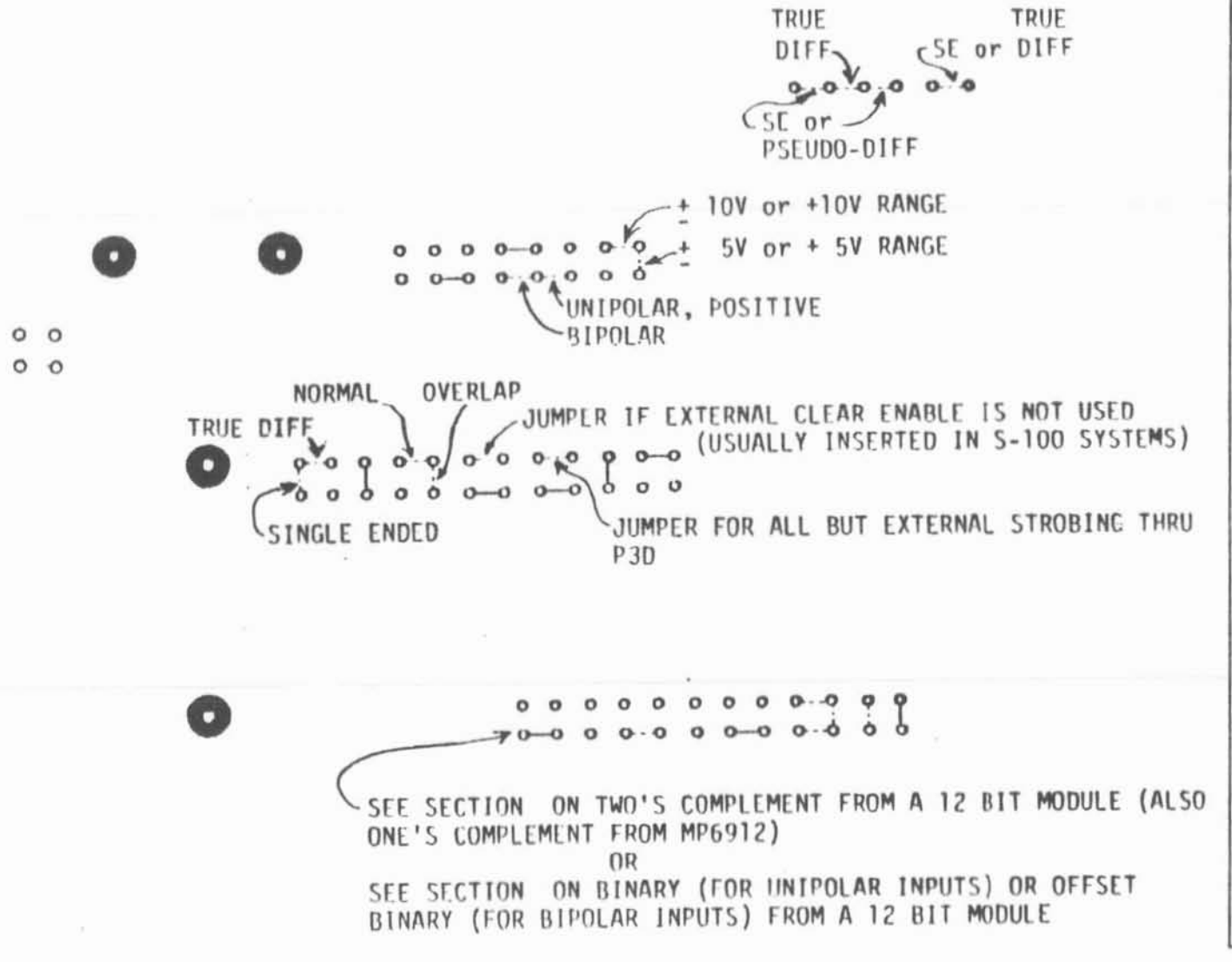
CONNECTOR BETWEEN MOTHER AND DAUGHTER BOARD (VIEWED FROM COMPONENT SIDE OF MOTHER BOARD)

P2-CONNECTOR PINOUTS (CONNECTOR BETWEEN MOTHER AND DAUGHTER BOARDS)

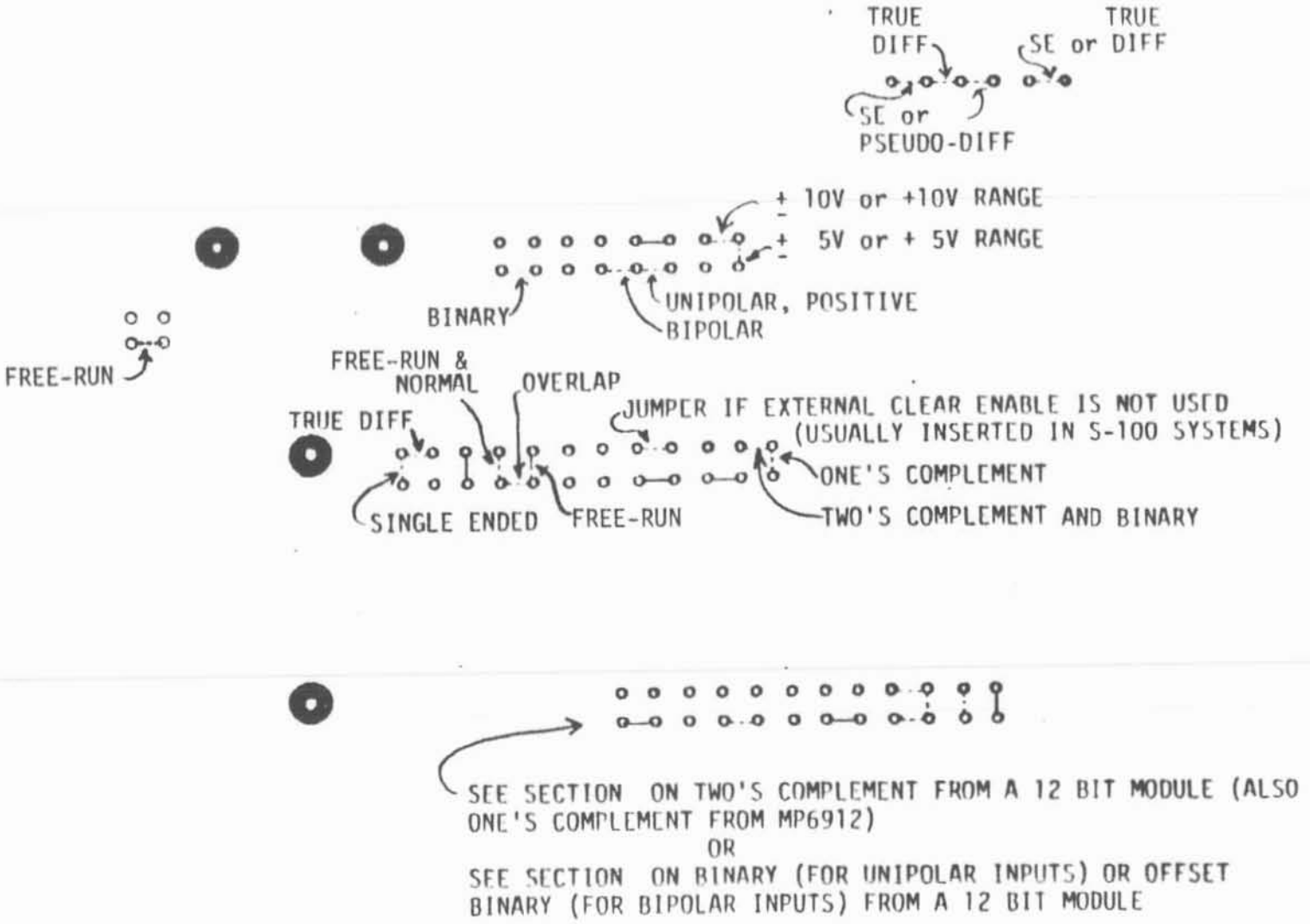
Pin Number	Function
1	GSO
2	LOAD EN
3	STROBE
4	GS1
5	MUX ADDR IN 1
6	MUX ADDR IN 2
7	MUX ADDR IN 4
8	MUX ADDR IN 8
9	MUX ADDR OUT 16
10	MUX ADDR OUT 32
11	MUX ADDR OUT 64
12	MUX ADDR OUT 128
13	EOC
14	BIT 15
15	BIT 14
16	BIT 13
17	BIT 12
18	BIT 11
19	BIT 10
20	BIT 9
21	BIT 8
22	MUX ADDR OUT 8
23	MUX ADDR OUT 4
24	MUX ADDR OUT 2
25	MUX ADDR OUT 1
26	CLEAR ENABLE
27, 28	+ 8 VOLTS
29, 30	- 20 VOLTS
31, 32	+ 20 VOLTS
33-42	GND.
43	BIT 7
44	BIT 6
45	BIT 5
46	BIT 4
47	BIT 3
48	BIT 2
49	BIT 1
50	BIT 0



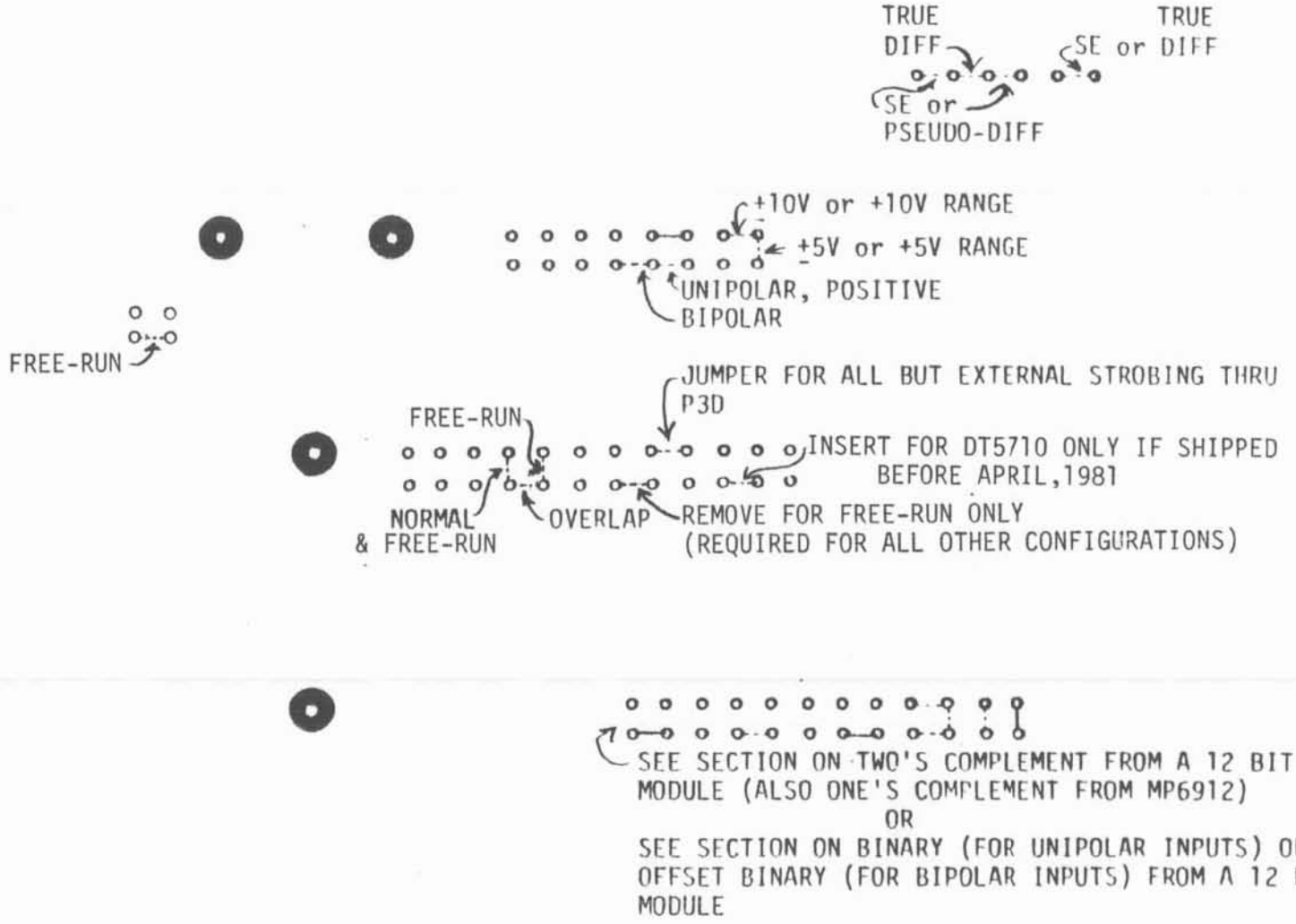
JUMPER ARLA NUMBERING—DAUGHTER BOARD


TRUE DIFF
TRUE SE or DIFF
SE or PSEUDO-DIFF
± 10V or +10V RANGE
± 5V or + 5V RANGE
UNIPOLAR, POSITIVE BIPOLAR
NORMAL
OVERLAP
TRUE DIFF
JUMPER IF EXTERNAL CLEAR ENABLE IS NOT USED (USUALLY INSERTED IN S-100 SYSTEMS)
SINGLE ENDED
JUMPER FOR ALL BUT EXTERNAL STROBING THRU P3D
SEE SECTION ON TWO'S COMPLEMENT FROM A 12 BIT MODULE (ALSO ONE'S COMPLEMENT FROM MP6912)
OR
SEE SECTION ON BINARY (FOR UNIPOLAR INPUTS) OR OFFSET BINARY (FOR BIPOLAR INPUTS) FROM A 12 BIT MODULE

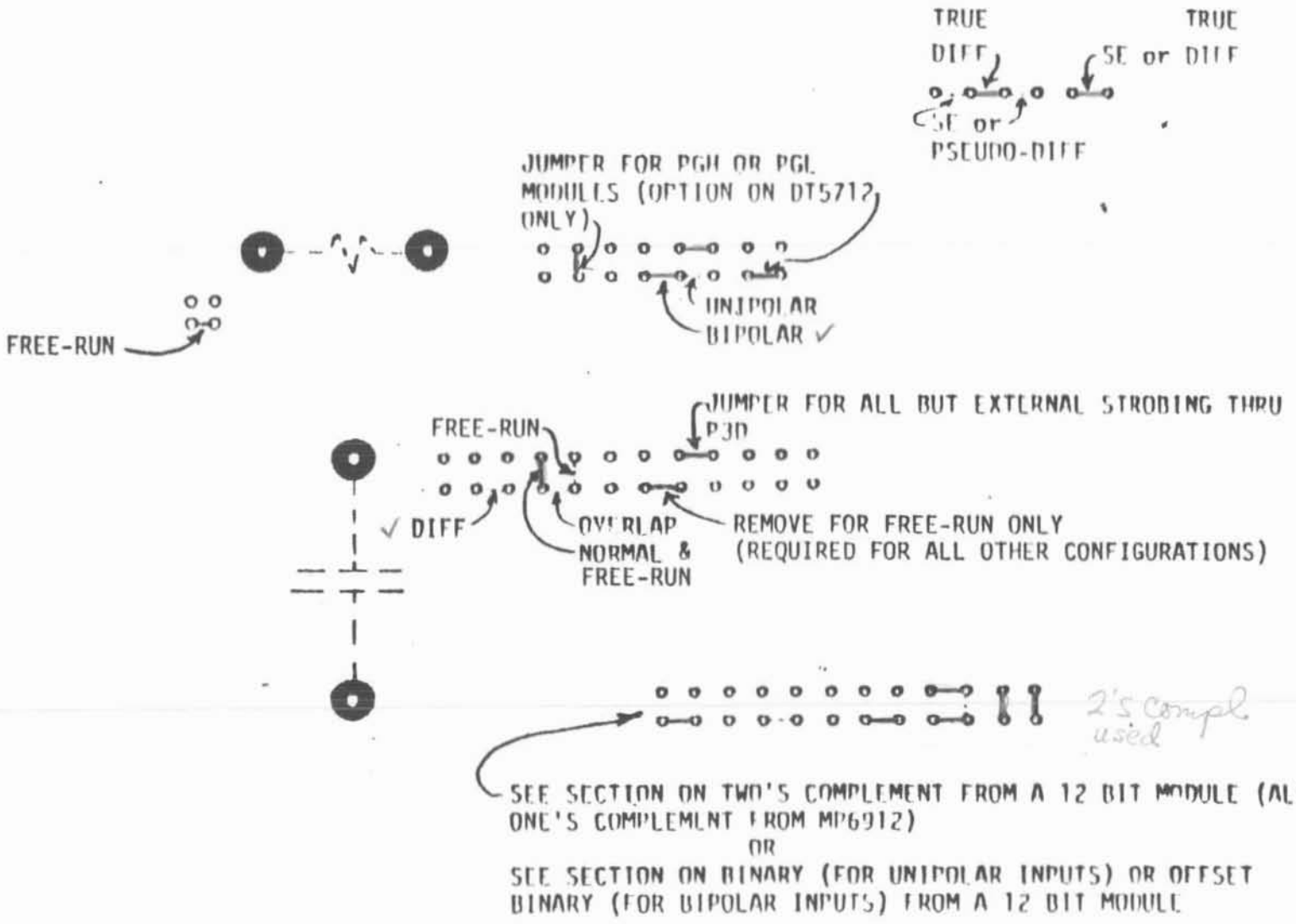
JUMPERING FOR MP6812 MODULE


TRUE DIFF
TRUE SE or DIFF
SE or PSEUDO-DIFF
± 10V or +10V RANGE
± 5V or + 5V RANGE
BINARY
UNIPOLAR, POSITIVE BIPOLAR
FREE-RUN
FREE-RUN & NORMAL
OVERLAP
JUMPER IF EXTERNAL CLEAR ENABLE IS NOT USED (USUALLY INSERTED IN S-100 SYSTEMS)
TRUE DIFF
ONE'S COMPLEMENT
SINGLE ENDED
FREE-RUN
TWO'S COMPLEMENT AND BINARY
SEE SECTION ON TWO'S COMPLEMENT FROM A 12 BIT MODULE (ALSO ONE'S COMPLEMENT FROM MP6912)
OR
SEE SECTION ON BINARY (FOR UNIPOLAR INPUTS) OR OFFSET BINARY (FOR BIPOLAR INPUTS) FROM A 12 BIT MODULE

JUMPERING FOR MP6912 MODULE

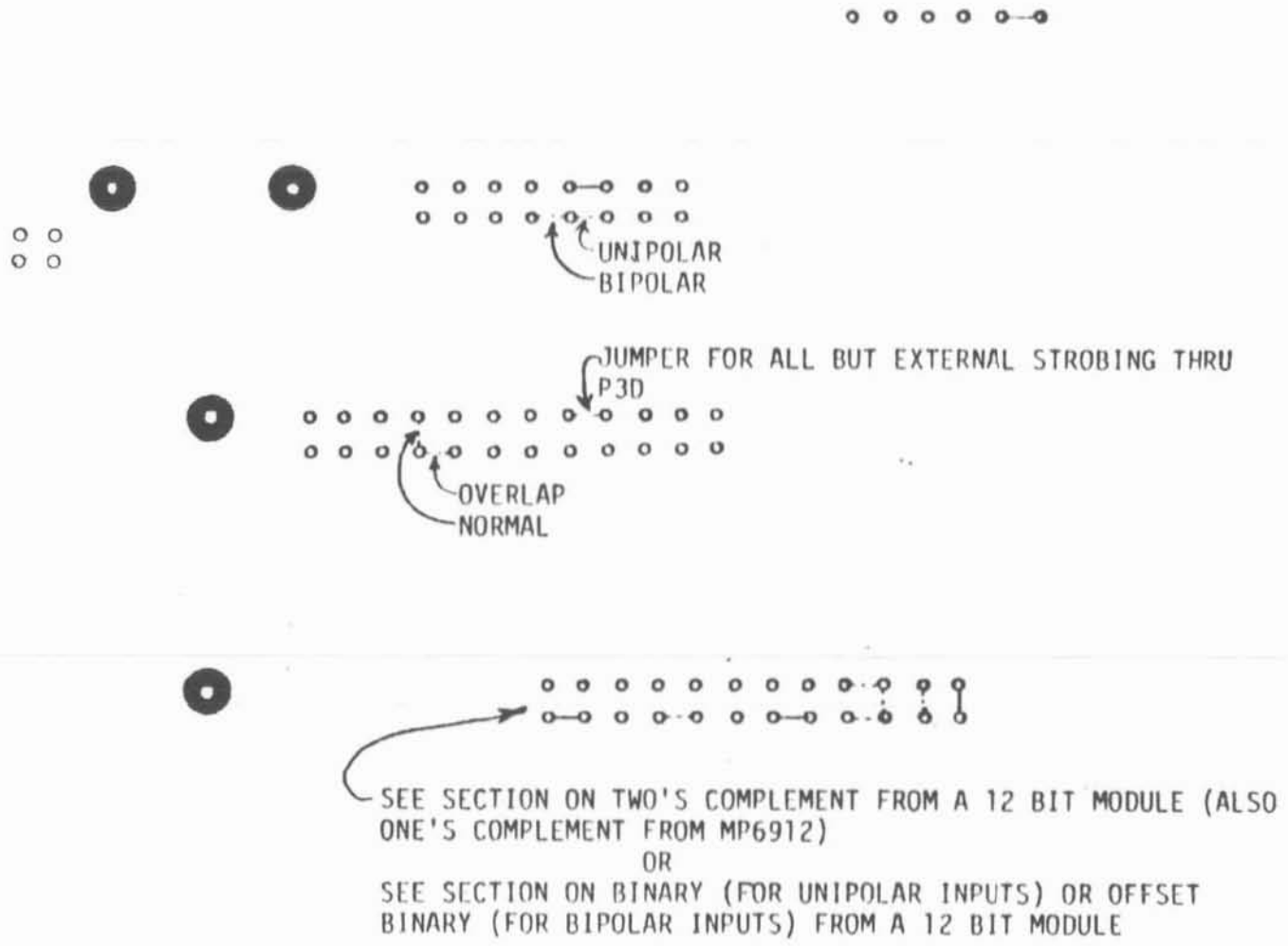

TRUE DIFF
TRUE SE or DIFF
SE or PSEUDO-DIFF
+10V or +10V RANGE
±5V or +5V RANGE
UNIPOLAR, POSITIVE
BIPOLAR
FREE-RUN
JUMPER FOR ALL BUT EXTERNAL STROBING THRU P3D
FREE-RUN
INSERT FOR DT5710 ONLY IF SHIPPED BEFORE APRIL,1981
NORMAL & FREE-RUN
OVERLAP
REMOVE FOR FREE-RUN ONLY (REQUIRED FOR ALL OTHER CONFIGURATIONS)
SEE SECTION ON TWO'S COMPLEMENT FROM A 12 BIT MODULE (ALSO ONE'S COMPLEMENT FROM MP6912)
OR
SEE SECTION ON BINARY (FOR UNIPOLAR INPUTS) OR OFFSET BINARY (FOR BIPOLAR INPUTS) FROM A 12 BIT MODULE

JUMPERING FOR DT5701 AND DT5710 MODULES

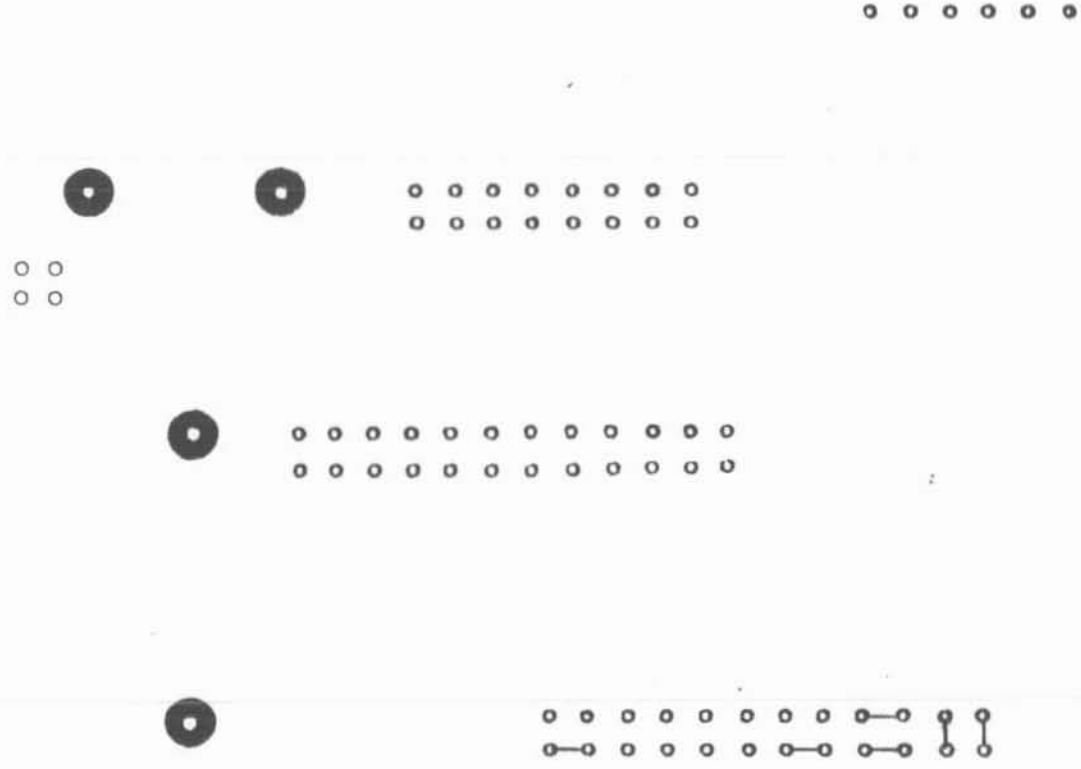

TRUE DIFF
TRUE SE or DIFF
SE or PSEUDO-DIFF
JUMPER FOR PGH OR PGL MODULES (OPTION ON DT5712 ONLY)
UNIPOLAR
BIPOLAR ✓
FREE-RUN
JUMPER FOR ALL BUT EXTERNAL STROBING THRU P3D
FREE-RUN
✓ DIFF
OVERLAP NORMAL & FREE-RUN
REMOVE FOR FREE-RUN ONLY (REQUIRED FOR ALL OTHER CONFIGURATIONS)
2's compl used
SEE SECTION ON TWO'S COMPLEMENT FROM A 12 BIT MODULE (ALSO ONE'S COMPLEMENT FROM MP6912)
OR
SEE SECTION ON BINARY (FOR UNIPOLAR INPUTS) OR OFFSET BINARY (FOR BIPOLAR INPUTS) FROM A 12 BIT MODULE

THIS one

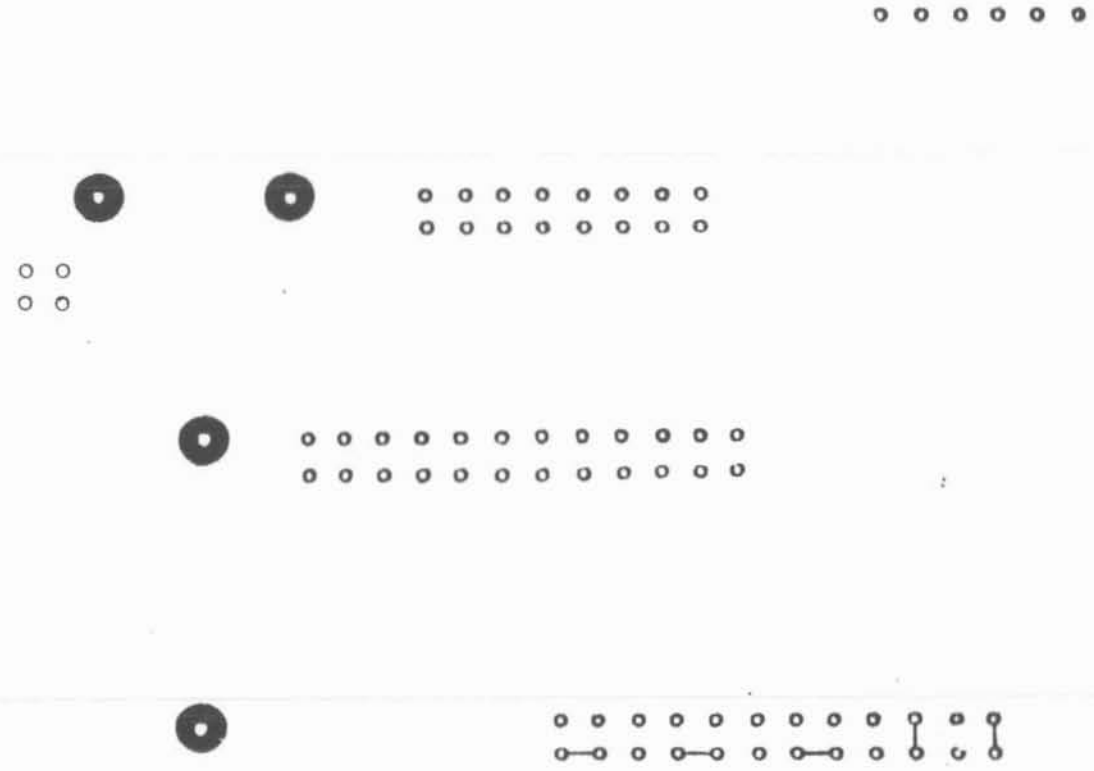
JUMPERING FOR DT5712 AND DT5702 MODULES


UNIPOLAR
BIPOLAR
JUMPER FOR ALL BUT EXTERNAL STROBING THRU P3D
OVERLAP
NORMAL
SEE SECTION ON TWO'S COMPLEMENT FROM A 12 BIT MODULE (ALSO ONE'S COMPLEMENT FROM MP6912)
OR
SEE SECTION ON BINARY (FOR UNIPOLAR INPUTS) OR OFFSET BINARY (FOR BIPOLAR INPUTS) FROM A 12 BIT MODULE

JUMPERING FOR DT5703 MODULES



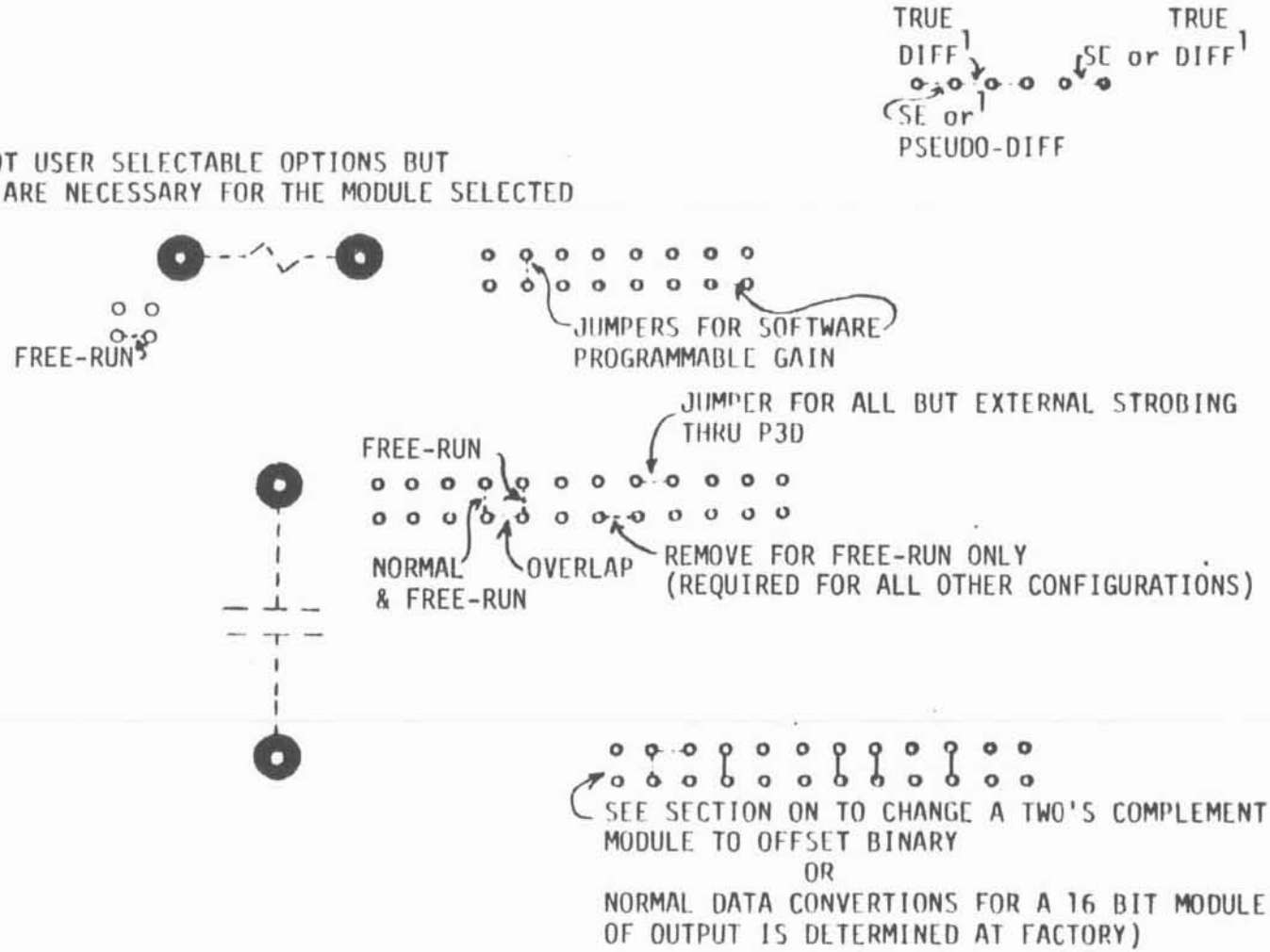
TWO'S COMPLEMENT FROM A 12 BIT MODULE (ALSO ONE'S COMPLEMENT FROM MP6912)



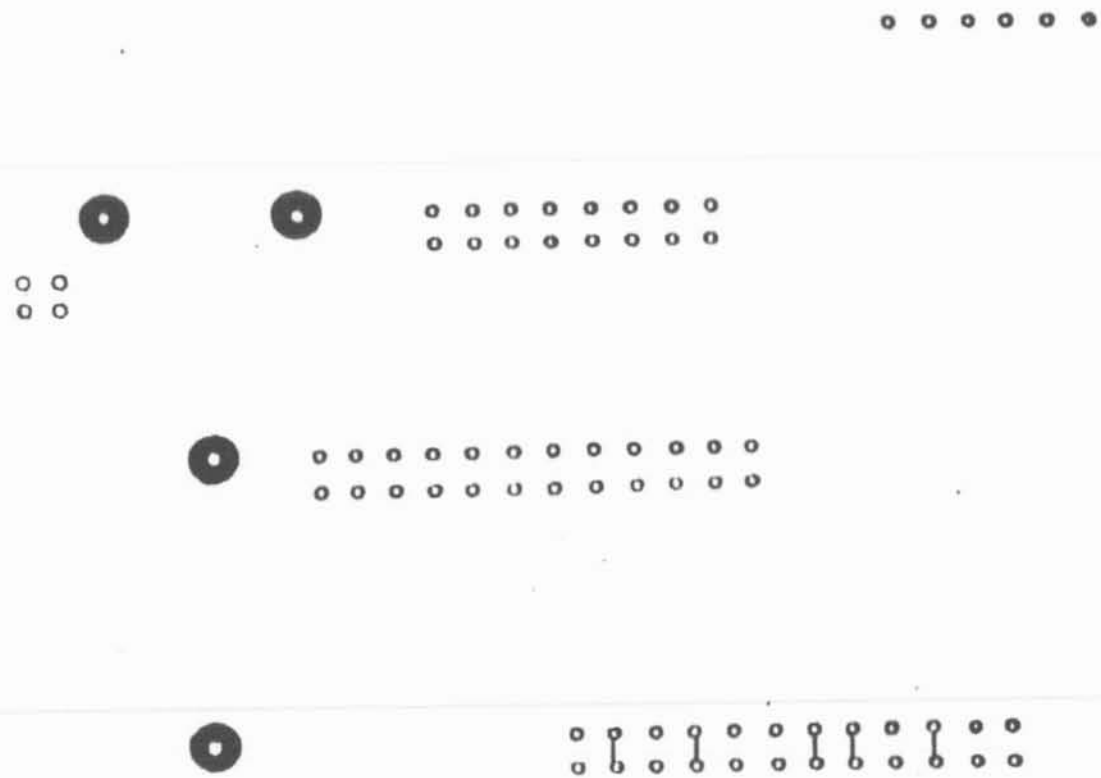
BINARY (FOR UNIPOLAR INPUTS) OR OFFSET BINARY (FOR BIPOLAR INPUTS) FROM A
12 BIT MODULE (ALL NUMBERS ARE POSITIVE, 16 BIT TO THE COMPUTER)

NOTES:

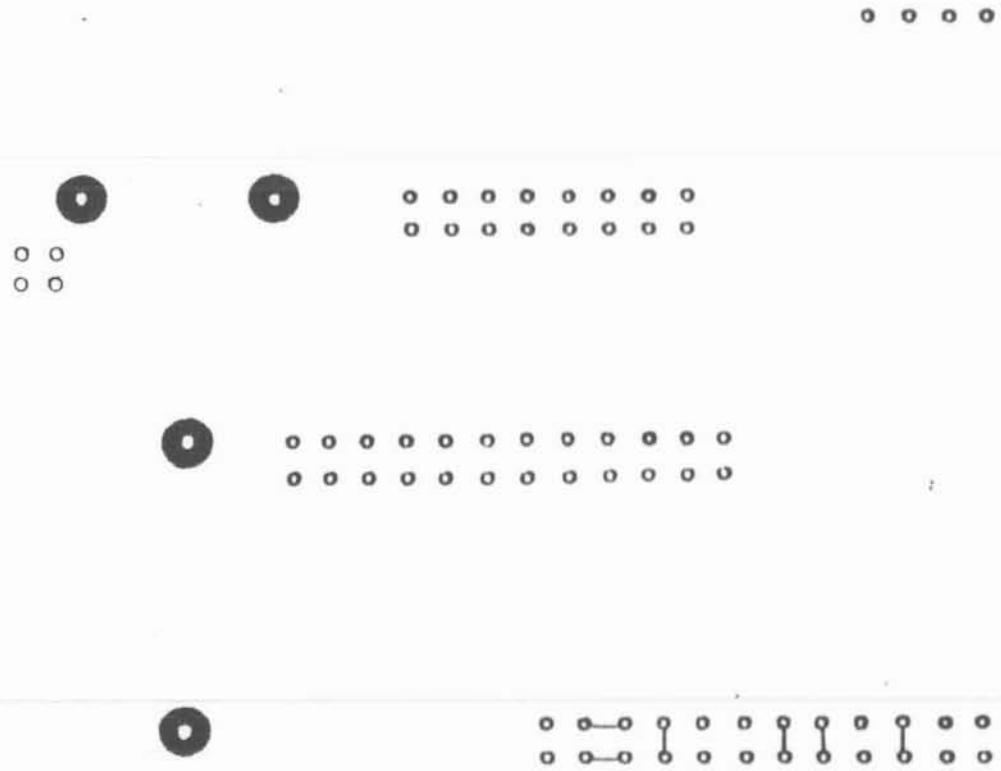
1 THESE ARE NOT USER SELECTABLE OPTIONS BUT THE JUMPERS ARE NECESSARY FOR THE MODULE SELECTED


TRUE DIFF[1]
TRUE SE or DIFF[1]
SE or[1] PSEUDO-DIFF
FREE-RUN
JUMPERS FOR SOFTWARE PROGRAMMABLE GAIN
JUMPER FOR ALL BUT EXTERNAL STROBING THRU P3D
FREE-RUN
NORMAL & FREE-RUN
OVERLAP
REMOVE FOR FREE-RUN ONLY (REQUIRED FOR ALL OTHER CONFIGURATIONS)
SEE SECTION ON TO CHANGE A TWO'S COMPLEMENT 16 BIT MODULE TO OFFSET BINARY
OR
NORMAL DATA CONVERTIONS FOR A 16 BIT MODULE (CHOICE OF OUTPUT IS DETERMINED AT FACTORY)

JUMPERING FOR DT5714 MODULE



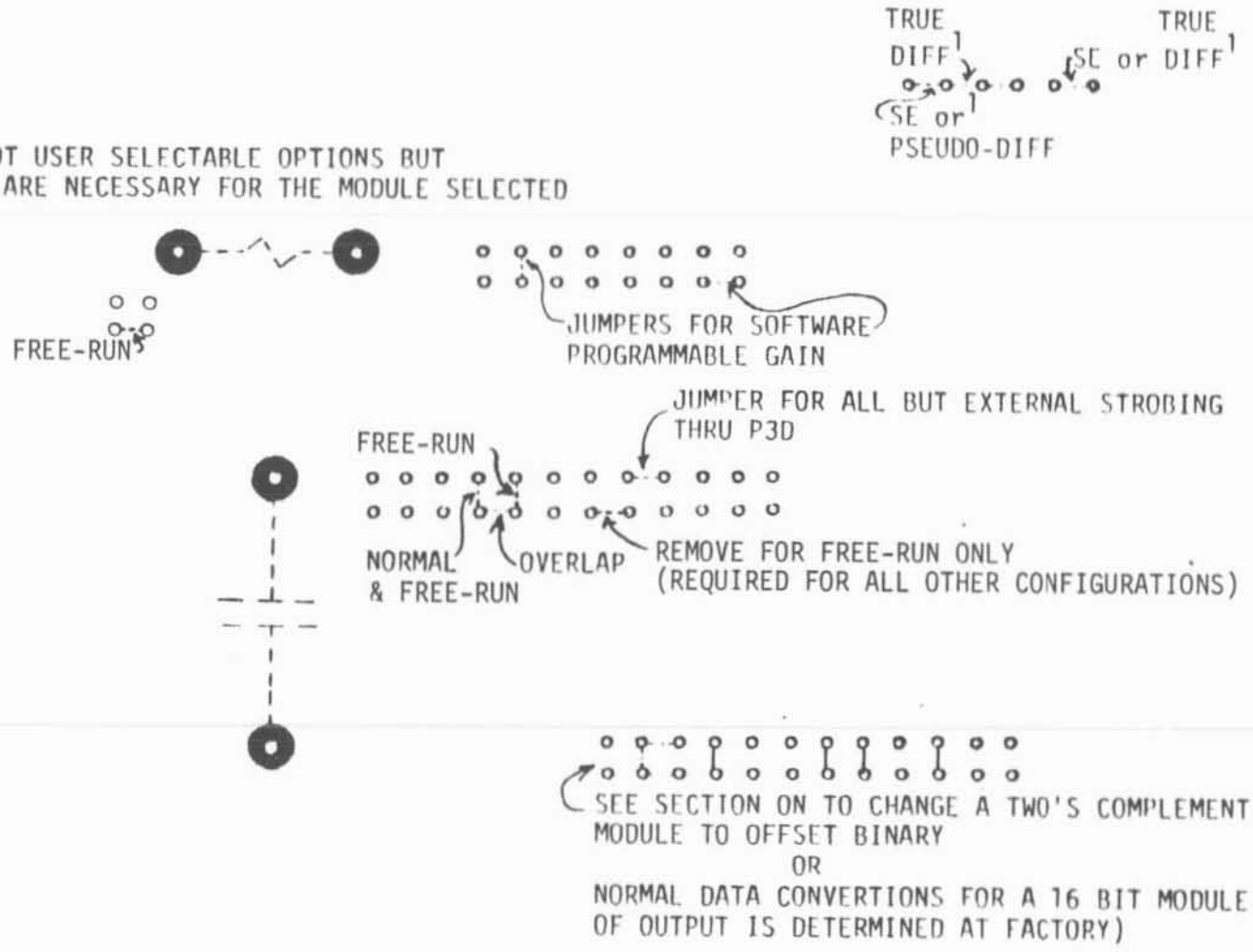
NORMAL DATA CONVERSIONS FOR A 14 BIT MODULE (CHOICE OF OUTPUT CODE IS DETERMINED AT FACTORY)



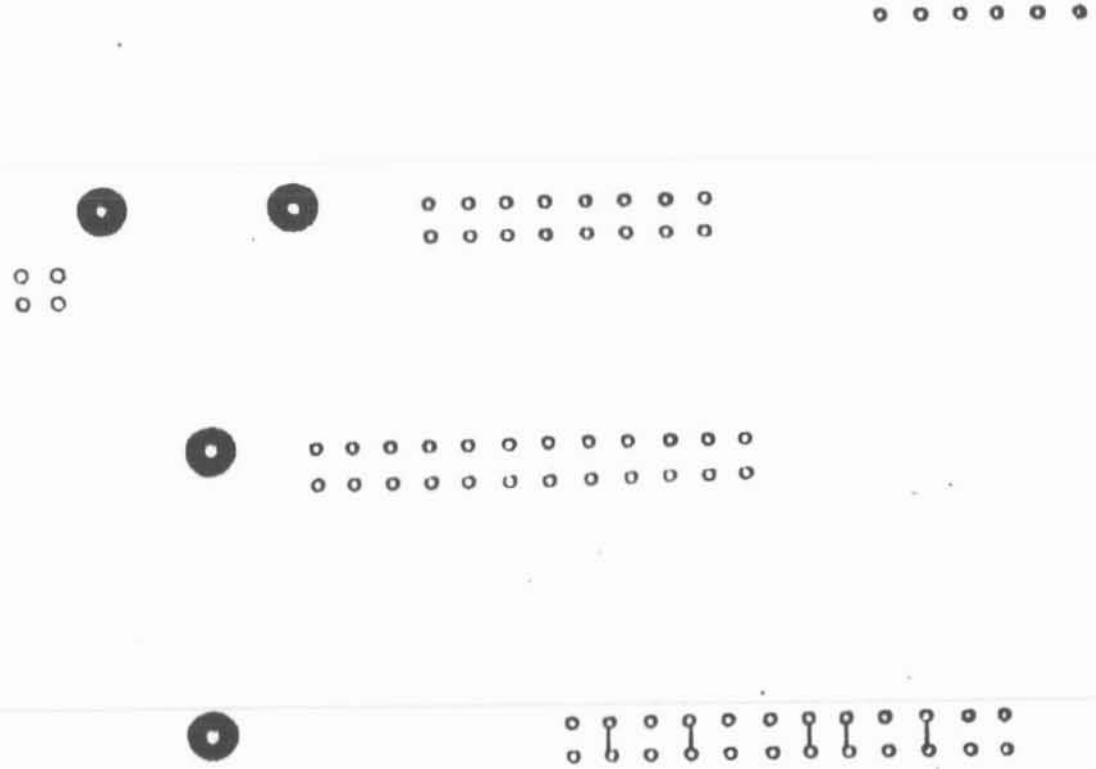
TO CHANGE A TWO'S COMPLEMENT 14 BIT MODULE TO OFFSET BINARY

NOTES:

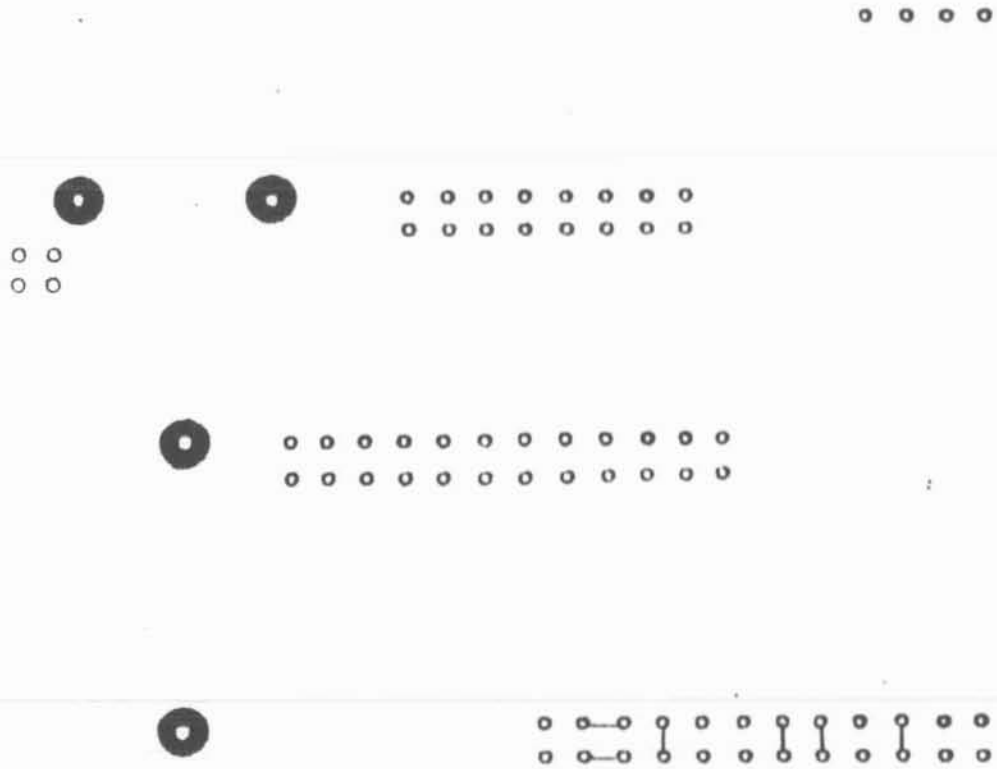
1 THESE ARE NOT USER SELECTABLE OPTIONS BUT THE JUMPERS ARE NECESSARY FOR THE MODULE SELECTED


TRUE DIFF 1
TRUE SE or DIFF 1
SE or 1 PSEUDO-DIFF
FREE-RUN
JUMPERS FOR SOFTWARE PROGRAMMABLE GAIN
JUMPER FOR ALL BUT EXTERNAL STROBING THRU P3D
FREE-RUN
NORMAL & FREE-RUN
OVERLAP
REMOVE FOR FREE-RUN ONLY (REQUIRED FOR ALL OTHER CONFIGURATIONS)
SEE SECTION ON TO CHANGE A TWO'S COMPLEMENT 16 BIT MODULE TO OFFSET BINARY
OR
NORMAL DATA CONVERTIONS FOR A 16 BIT MODULE (CHOICE OF OUTPUT IS DETERMINED AT FACTORY)

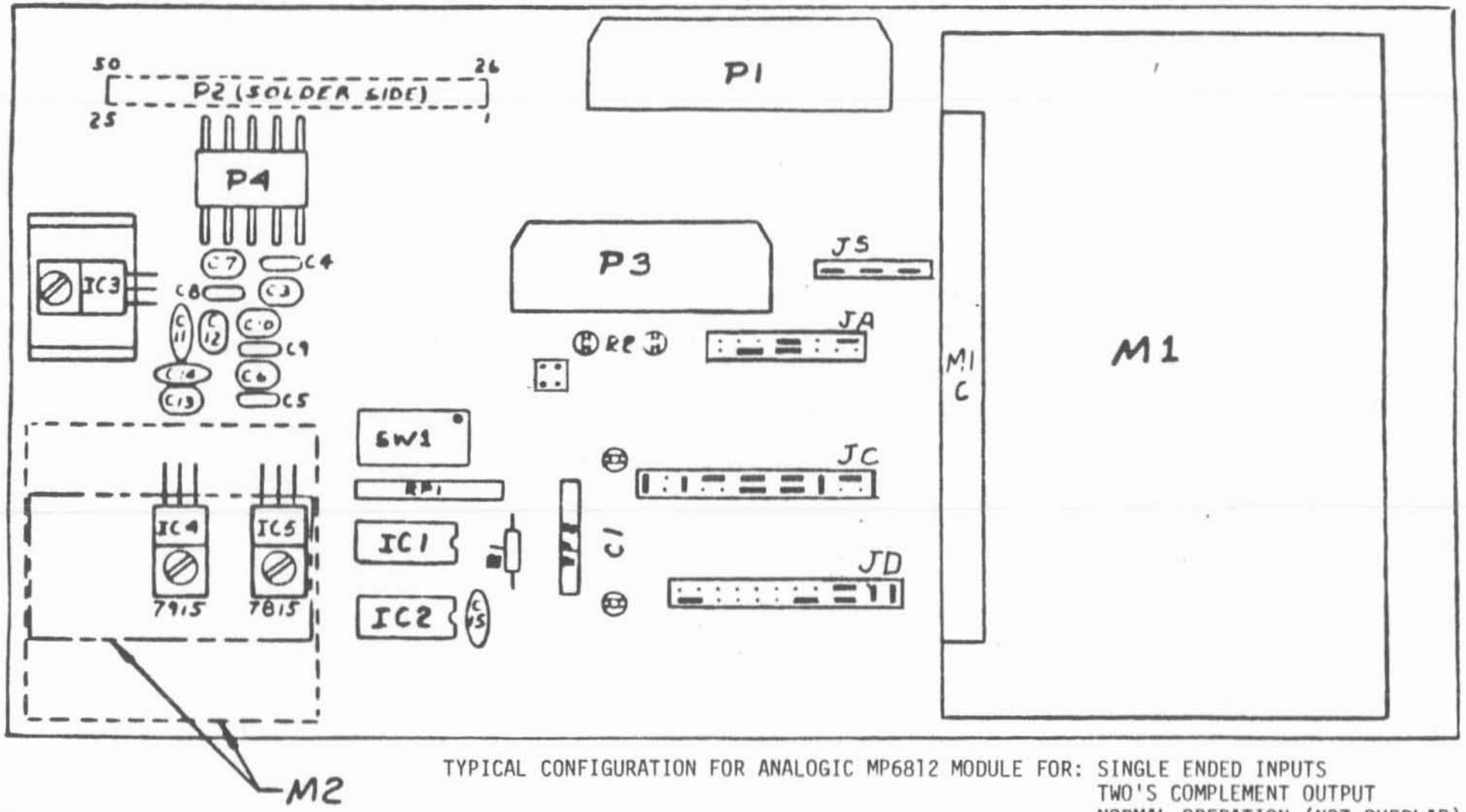
JUMPERING FOR DT5716 MODULE



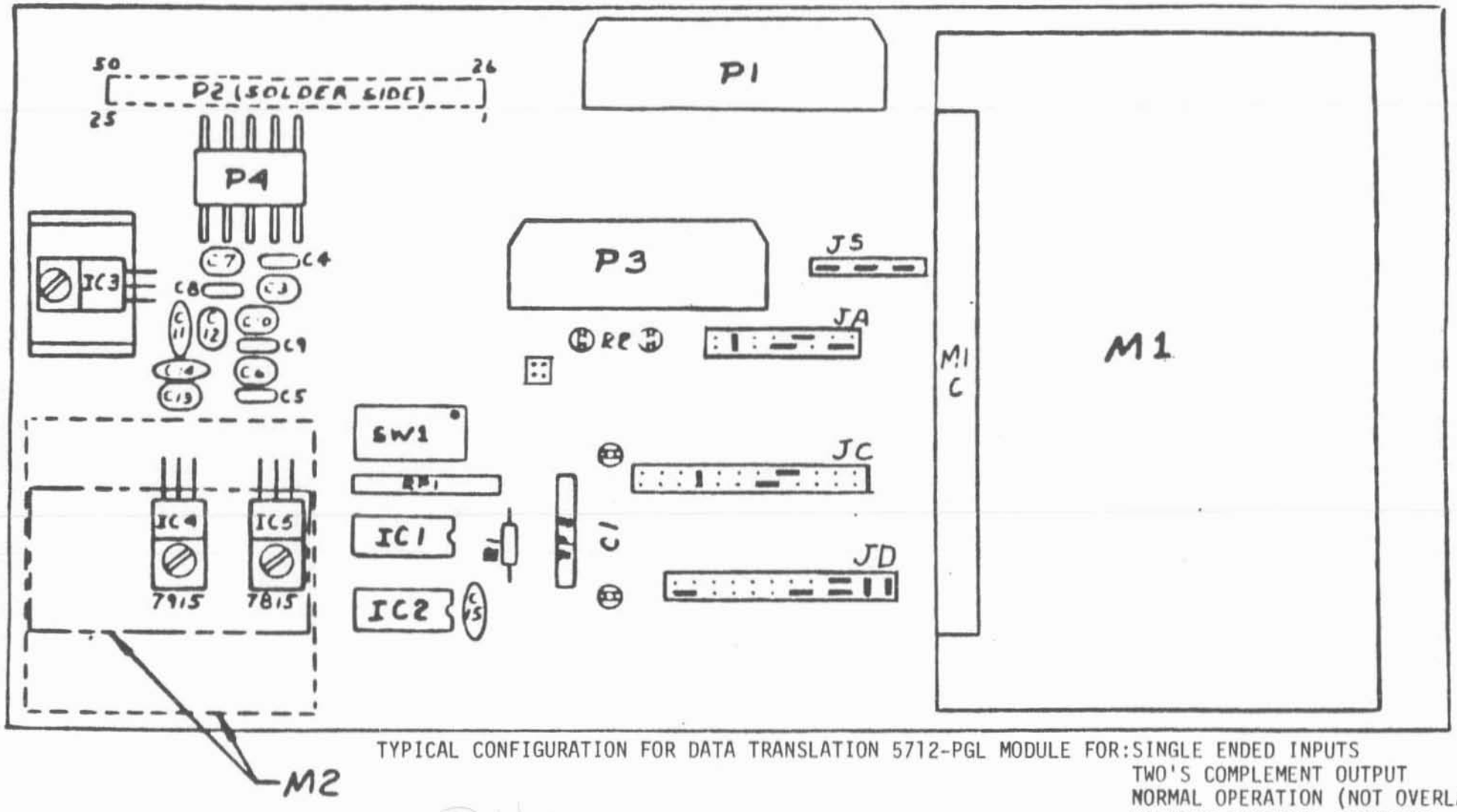
NORMAL DATA CONVERSIONS FOR A 16 BIT MODULE (CHOICE OF OUTPUT CODE IS DETERMINED AT FACTORY)



TO CHANGE A TWO'S COMPLEMENT 16 BIT MODULE TO OFFSET BINARY

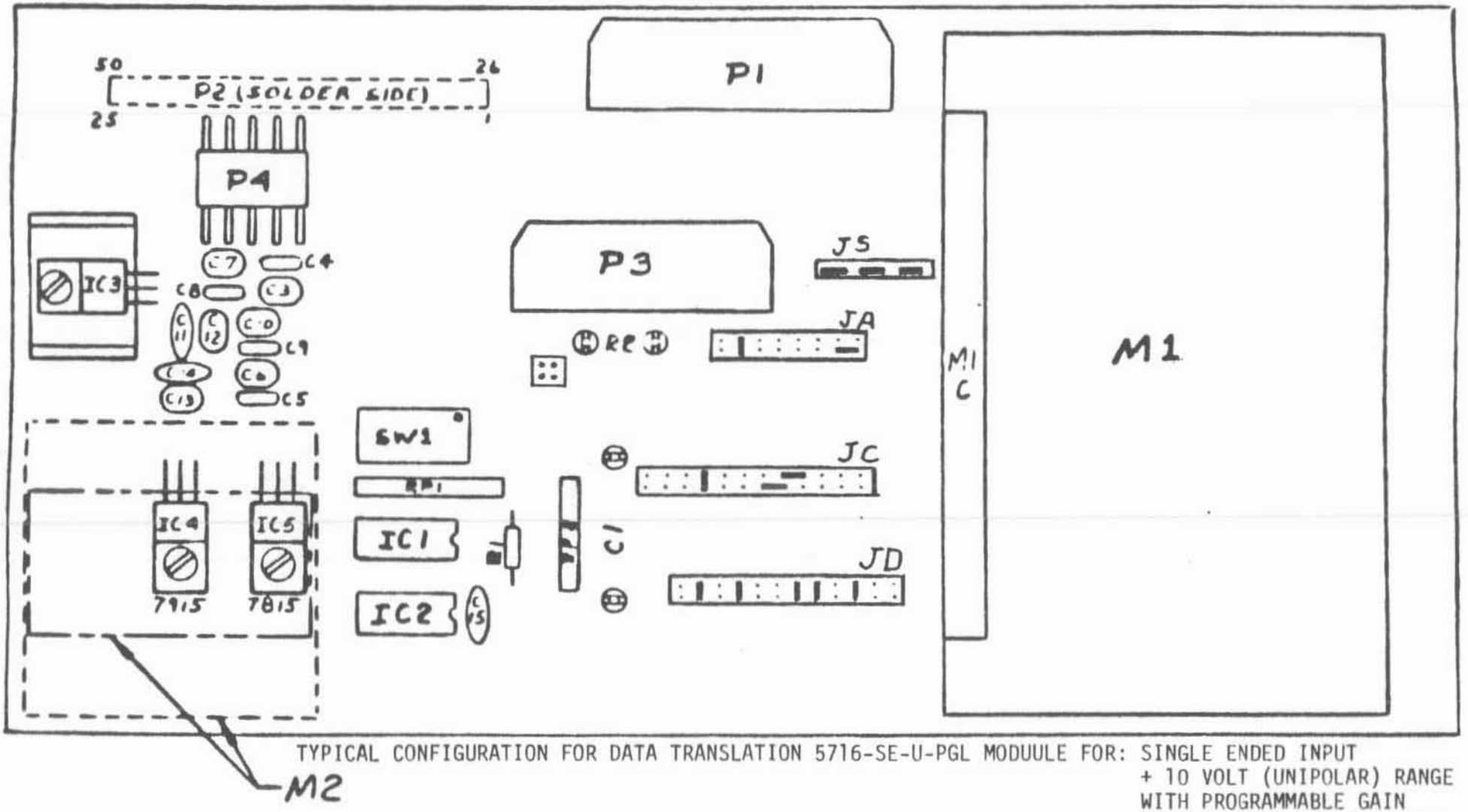


TYPICAL CONFIGURATION FOR ANALOGIC MP6812 MODULE FOR: SINGLE ENDED INPUTS
TWO'S COMPLEMENT OUTPUT
NORMAL OPERATION (NOT OVERLAP)
WITHOUT EXTERNAL STROBING THRU P3D
± 10 VOLT (BIPOLAR) RANGE

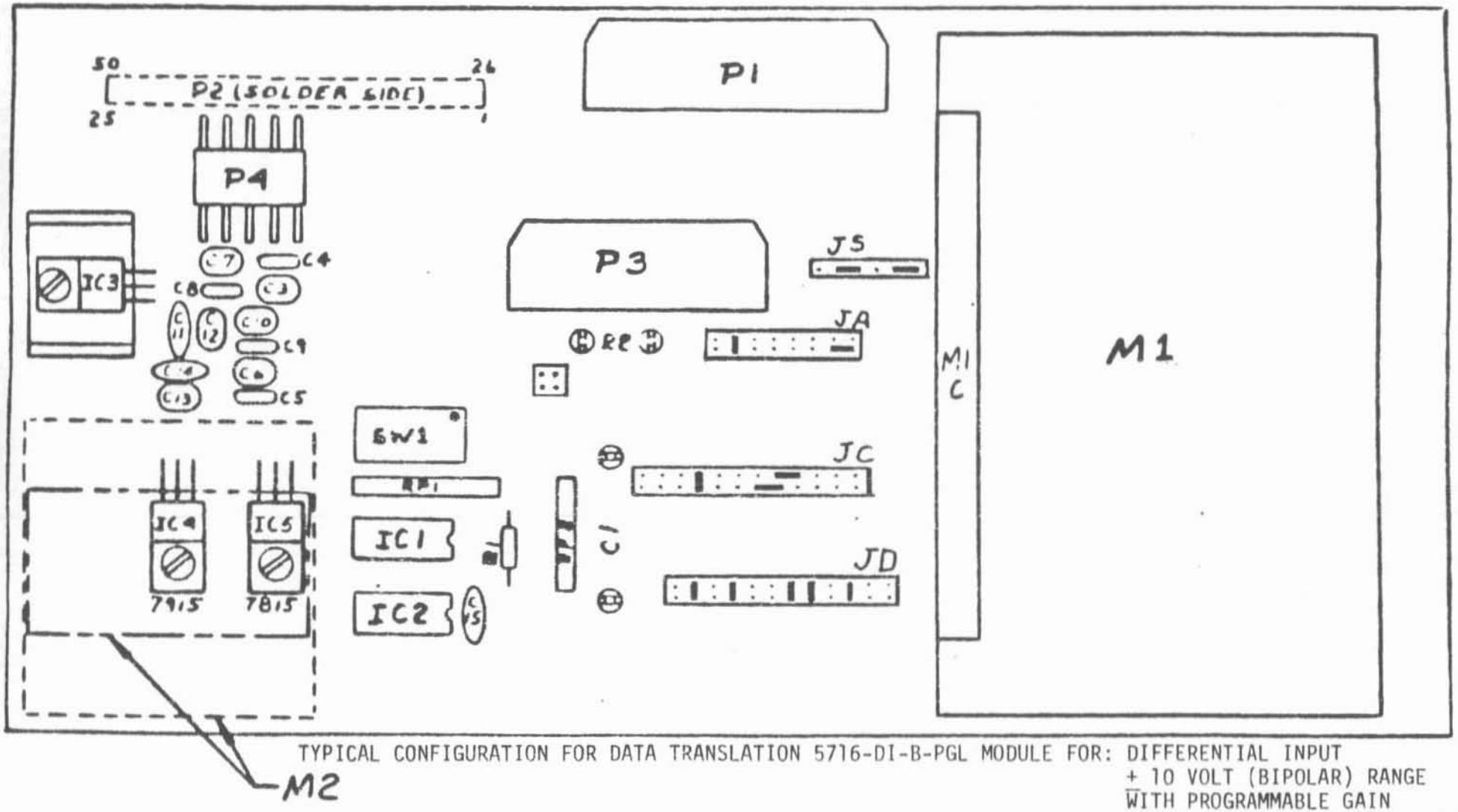


TYPICAL CONFIGURATION FOR DATA TRANSLATION 5712-PGL MODULE FOR: SINGLE ENDED INPUTS
TWO'S COMPLEMENT OUTPUT
NORMAL OPERATION (NOT OVERLAP)
WITHOUT EXTERNAL STROBING
THRU P3D
WITH PROGRAMMABLE GAIN
± 10 VOLT (BIPOLAR) RANGE

THIS one



TYPICAL CONFIGURATION FOR DATA TRANSLATION 5716-SE-U-PGL MODUULE FOR: SINGLE ENDED INPUT
+ 10 VOLT (UNIPOLAR) RANGE
WITH PROGRAMMABLE GAIN
NORMAL OPERATION (NOT OVERLAP)
WITHOUT EXTERNAL STROBING THRU P3D
TWO'S COMPLEMENT OUTPUT



TYPICAL CONFIGURATION FOR DATA TRANSLATION 5716-DI-B-PGL MODULE FOR: DIFFERENTIAL INPUT
+ 10 VOLT (BIPOLAR) RANGE
WITH PROGRAMMABLE GAIN
NORMAL OPERATION (NOT. OVERLAP)
WITHOUT EXTERNAL STROBING
THRU P3D
TWO'S COMPLEMENT OUTPUT

PROGRAMMING THE S-100 AD212 BOARD

There are 16 I/O ports (or memory locations, depending on the board configuration) involved in communicating with the A/D. For 8 bit systems, these are configured to provide eight possible READ and WRITE operations with two possible interchangeable locations for each READ and WRITE. The READ and WRITE Register assignments are given following this section.

The generalized algorithm for sampling an A/D input is:

1) Set Command Port (Write Port 0 or 1) to desired options (gain select; auto sequence or load enable; external strobe enable; interrupt enable for timer 1,2, A/D overrun or A/D done; and WAIT function enable).

2) Set multiplexer address to desired input line (0 through 256). Write port 2 or 3 .

3) Start conversion. Output (or store) anything to this port. (Write port 4 or 5).

4) Read status of A/D. This is bit 7 of READ port 0 or 1. It is designated A/D DONE and will become 1 when the conversion is complete.

5) Read low 8 bits of A/D from Read port 2 or 3.

6) Read high 8 bits of A/D from Read port 4 or 5.

The timer can be controlled as follows:

To write to the Data Port of the AM9513 timer, use WRITE REGISTER C or D.

To write to the Command Port of the AM9513 timer, use WRITE REGISTER E or F.

To read from the Data Port of the AM9513 timer, use READ REGISTER C or D.

To read from the Command Port of the AM9513 timer, use READ REGISTER E or F.

To clear timer flop 1, write to WRITE REGISTER 6 or 7.

To clear timer flop 2, write to WRITE REGISTER 8 or 9.

The other function controlled through software is as follows:

To clear the overrun flop, write to WRITE REGISTER A or B.

The Register Assignments are given on the next two pages.

WRITE

0 or 1 COMMAND							
INT ENABLE A/D DONE	INT ENABLE A/D OVERRUN	INT ENABLE TIMER FLOP 2	INT ENABLE TIMER FLOP 1	0-RUN[1] 1-STOP[1] 1-EXTERNAL[2] STROBE ENABLE	0 FOR AUTO SEQUENCE 1 FOR LOAD ENABLE	GAIN SELECT 1	GAIN SELECT 0
7	6	5	4	3	2	1	0
2 or 3 MUXADDR TO A/D							
128	64	32	16	8	4	2	1

(ALSO USED FOR WAIT FUNCTION ENABLE)

4 or 5	WRITING TO THIS PORT STROBES (STARTS) THE A/D
6 or 7	WRITING TO THIS PORT CLEARS TIMER FLOP 1
8 or 9	WRITING TO THIS PORT CLEARS TIMER FLOP 2
A or B	WRITING TO THIS PORT CLEARS THE OVERRUN FLOP
C or D	DATA PORT OF AM9513
E or F	COMMAND PORT OF AM9513

GAIN DETERMINATION

BIT 1	BIT 0	PGL GAIN	PGH GAIN
0	0	1	1
0	1	10	2
1	0	100	4
1	1	500	8

REGISTER ASSIGNMENTS

1 IF JUMPERED FOR FREE-RUN FEATURE

2 IF JUMPERED FOR EXTERNAL STROBE

READ

0 or 1 STATUS

7	6	5	4	3	2	1	0
A/D DONE	A/D OVERRUN	TIMER INT 2	TIMER INT 1	8	4	2	1

MUX ADDRESS CURRENTLY IN A/D

2 or 3 LOW 8 BITS OF A/D
READING THIS PORT WILL CAUSE THE CPU TO WAIT FOR END OF CONVERSION IN THE READY LINE SWITCH (SW3-6) IS IN AND THE WAIT BIT IS SET.

4 or 5 HIGH 8 BITS OF A/D or 16 BITS OF A/D
READING THIS PORT WILL RESET THE DONE BIT AUTOMATICALLY. IF THE OVERRUN BIT IS USED THEN THIS PORT MUST ALWAYS BE READ AFTER PORT 2

0, 7, 8, 9, A, B ARE NOT USED

C or D DATA PORT OF AM9513

E or F COMMAND PORT OF AM9513

REGISTER ASSIGNMENTS

BASIC program examples follow.

The following programs assume the board is set up for:

1. I/O mapped operation
2. For an 8 bit system (conventional S100 system)
3. Utilizes status test of A/D
4. Starting location 16_D (10_H)
5. No wait state generation
6. No interrupts

TIME OF DAY

The following BASIC program:

SETS UP THE AMD 9513 TIMER I.C. FOR TIME OF DAY OPERATION.

The initial time and day is inserted at the locations marked by a "*" in the program. These values are the decimal equivalents of the values indicated, in HEX form. For example, in line 90, if the initial value of the seconds is to be 30, the number used in the program would be 48. Nine seconds would be a 9 in the program and 43 seconds would be a 67 in the program.

BASIC:

		HEX	
10	OUT(30)=255	FF	Master Mode Reset
20	OUT(30)=23	17	Set Data Pointer to Master Mode Register
30	OUT(28)=255	FF	Set Master Mode Register to:BCD,
40	OUT(28)=138	8A	Data Pointer Increment, 8 Bit Bus, FOUT ON, FOUT ÷ 10, FOUT SOURCE F5, Compare 1 & 2 Enabled, TOD Enabled ÷ 10
50	OUT(30)=01	01	Set Data Pointer to Counter Mode-Register 1
60	OUT(28)=57	39	Set Counter Mode to: SOURCE=F5,
70	OUT(28)=15	0F	ACTIVE HI TC, BCD, COUNT UP
80	OUT(28)=*		Tenths and Hundreths-Seconds
90	OUT(28)=*		Tens and Ones-Seconds
100	OUT(30)=02	02	Set Data Pointer to Counter Mode Register 2
110	OUT(28)=61	3D	Set counter Mode to: SOURCE=TC1,
120	OUT(28)=00	00	ACTIVE LO TC, BCD, COUNT UP
130	OUT(28)=*		Tens and Ones-Minutes
140	OUT(28)=*		Tens and Ones-Hours
150	OUT(30)=03	03	Set Data Pointer to Counter Mode Register 3.
160	OUT(28)=57	39	Set Counter Mode to:SOURCE=TC2,
170	OUT(280=00	00	ACTIVE HI TC, BCD, COUNT UP
180	OUT(28)=*		Tens and Ones-Days
190	OUT(28)=*		Thousands and Hundreds-Days
200	OUT(30)=67	43	Load Counter 1 and 2 with Contents of Load Registers

```
                                  HEX
210  OUT(30)=09                   09        Set Load Register of Counter #1
                                            to Zero
220  OUT(28)=00                   00
230  OUT(28)=00                   00
240  OUT(30)=10                   0A        Set Load Register of Counter #2
                                            to Zero
250  OUT(28)=00                   00
260  OUT(28)=00                   00
270  OUT(30)=68                   44        Load Counter #3 from Load Register
280  OUT(30)=39                   27        Arm Counters 1, 2, 3
290  STOP
```

The following BASIC program:

CONTINUOUSLY SAVES, INPUTS, AND PRINTS THE CONTENTS OF THE
TIME OF DAY REGISTERS

```
500  OUT(30)=167                    167D=A7H. Save Counters 1, 2, 3
510  OUT(30)=17                     Set Data Pointer to Counter #1,
                                    HOLD Register
520  A=IN(28)                       INPUT Tenths and Hundreths-Seconds
530  B=IN(28)                       INPUT Tens and Ones-Seconds
540  IF (A#0)+(B#0) GOTO 560        Check for Possible Ripple Carry Error
550  OUT(30)=166                    166=A6H. IF error possible, Resave
                                    counters 2, 3
560  OUT(30)=18                     Set Data Pointer to Counter #2,
                                    HOLD Register
570  C=IN(28)                       INPUT Tens and Ones-Minutes
580  D=IN(28)                       INPUT Tens and Ones-Hours
590  OUT(30)=19                     Set Data Pointer to Counter #3
600  E=IN(28)                       INPUT Tens and Ones-Days
610  F=IN(28)                       INPUT Thousand and Hundreds-Days
620  PRINT#%,F,E,,D,,C,,B,,A        Print out values in HEX
630  GOTO 500                       Jump Back to Beginning
```

ALARM REGISTER

The AMD 9513 contains two 16 bit alarm registers which are constantly compared with counter registers 1 and 2. When enabled, the outputs of the comparators take the place of the normal outputs of the counters, OUT1 and OUT2. The active level is determined by the setting of the output control, specified in bits 0, 1 and 2 of the individual Counter Mode Registers. Comparators 1 and 2 are enabled by a 1 in Bits 2 and 3 respectively in the Master Mode Register. In the special case that both comparators are enabled and the time of day function has been enabled, OUT2 will be the output of a full 32 bit comparison of both alarm registers with their respective counters. Since the counter registers have accuracy to hundreths of a second, it is impossible to detect a true comparator output condition in BASIC using the 32 bit comparison option, becasue the comparator output will only be true for .01 seconds. The following programs demonstrate how to set up and use Alarm 2 for comparison of hours and minutes.

The following BASIC programs:

PRINTS THE COMPARATOR 2 STATUS. THE STATUS WILL BE A "1" UNTIL THE CLOCK REACHES THE TIME SPECIFIED IN THE ALARM REGISTERS, AT WHICH TIME THE STATUS WILL BECOME A "0". THE "0" WILL LAST FOR ONE MINUTE, THE TIME THAT COUNTER 2 AND ALARM REGISTER 2 ARE THE SAME.

The time is inserted at the locations marked by a "*" in the program. These values are the decimal equivalents of the values indicated, in HEX form. The time in these positions is set to the desired time for the alarm comparators to be true.

BASIC:

```
                                HEX
700  OUT(30)=23                 17      Set Data Pointer to Master Mode
                                        Register
710  QUT(28)=251                FB      Set Master Mode Register to Comparator
                                        1 Disable, Comparator 2 Enable
720  OUT(30)=15                 0F      Set Data Pointer to Alarm 2 Register

730  OUT(28)= *                         Tens and Ones-Minutes

740  OUT(28)= *                         Tens and Ones-Hours

750  STOP

800  X=IN(30)                           INPUT Status Byte

810  Y=X/4-(X/8)*2                      Isolate Bit 4, the Comparator 2 Output
                                        (Note: The technique used is for
                                        INTEGER BASIC only)
820  PRINT Y                            PRINT Output of Comparator 2

830  GOTO 800                           Go Back to Beginning
```

EVENT COUNTING

The following BASIC program will:

SETS UP COUNTER 4 OF THE TIMER TO COUNT RISING EDGES OF THE DATA COMING IN ON SRC1.

BASIC:

		HEX	
10	OUT(30)=200	C8	Disarm Counter 4
20	OUT(30)=04	04	Set Data Pointer to Counter 4, Counter Mode Register
30	OUT(28)=41	29	Set Counter Mode 4 to Count on Rising Edge: Count Source=SRC1, Binary
40	OUT(28)=01	01	Count, Count Up.
50	OUT(28)=00	00	Set Load Register, Counter 4, to Zero
60	OUT(28)=00	00	
70	OUT(30)=72	48	Load Counter 4 with Load Register
80	OUT(30)=40	28	Arm Counter
90	STOP		

The following BASIC program will:

READ THE VALUE IN TIMER 4 (TIMER 4 WILL BE COUNTING THE RISING EDGES OF THE DATA COMING IN ON SRC1)

BASIC:

200	OUT(30)=168	A8	Save Counter 4 in Hold Register
210	OUT(30)=20	14	Set Data Pointer to Hold Register 4
220	A=IN(28)		Input Lo and Hi byte of Hold Register 4
230	B=IN(28)		
240	C=B*256+A		Compute Total
250	PRINT C		PRINT Value in Register
260	GOTO 200		Go Back to Beginning

A/D OF SINGLE CHANNEL

The following BASIC program will:

CONTINUOUSLY CONVERT CHANNEL ZERO AND PRINT THE RESULTS ON THE TERMINAL.

BASIC:

```
10  OUT(16)=04                  Set Command to Load Enable,
                                No Auto Incrementing
20  OUT(18)=00                  Set Channel to 0

30  OUT(20)=00                  Start Conversion

40  IF IN(16)/128=0 GOTO 40     Wait for "DONE" bit

50  A=IN(18)                    INPUT Lo Byte

60  B=IN(20)                    INPUT Hi Byte

70  PRINT#%,B,A                 PRINT in Hex

80  GOTO 30                     Go Back and Repeat
```

Note: Line 40 makes special use of INTEGER BASIC to isolate the "DONE" Bit.

A/D WITH AUTO-INCREMENTING

The following BASIC program:

SETS THE BOARD TO THE AUTO-INCREMENT MODE, STARTING WITH CHANNEL 0 AND ENDING WITH CHANNEL 9. IT THEN PERFORMS CONTINUOUS CONVERSIONS, PRINTING 10 VALUES IN EACH ROW SO CHANNEL 0 IS IN THE FIRST COLUMN, CHANNEL 1 IN THE SECOND, ETC.

The switches on the daughter board are set to the last channel to be converted in the increment sequence. In this case a 9 (00001001). Lines 20 and 30 set the channel select address on the board to 255, which is necessary since in the auto-incrementing mode this address is automatically incremented before each conversion, making the first channel converted channel 0. The start conversion in line 30 is needed since the specified channel number is not acutally loaded into this register until a conversion is performed. Line 40 sets the register which holds the starting channel in the auto increment sequence to 0; therefore, after converting channel 9, the next channel converted will be 0.

BASIC:

```
10   OUT(16)=04                    Load Enable
20   OUT(18)=255                   Set Channel Number to 255
30   OUT(20)=00                    Start Conversion
40   OUT(18)=00                    Set Channel Number to 0
50   OUT(16)=00                    Enable Auto Incrementing
60   FOR X=0 TO 9                  9 is the Last Channel to be
                                   Converted
70   OUT(20)=00                    Start Conversion
80   IF IN(16)/128=0 GOTO 80       Wait for "DONE" bit.
90   A=IN(18)                      INPUT Lo Byte
100  B=IN(20)                      INPUT Hi Byte
110  PRINT#%,A,B,                  PRINT Values in Hex
120  NEXT X
130  PRINT                         End of Row
140  GOTO 60                       Go Back and Repeat Process
```

Note: Line 80 makes special use of INTEGER BASIC to isolate Bit 7 of the input byte.

TIMER CONTROL OF A/D

The following BASIC program:

SETS UP COUNTER 5 OF THE TIMER TO PUT OUT A PULSE ONCE PER SECOND AT OUT 5, AND THEN CONTINUOUSLY CHECKS THE A/D STATUS TO CHECK FOR A "DONE" (END OF CONVERSION) TO USE THIS OPTION.

A jumper must be connected between OUT 5 (Pin 4, connector P3) and the external trigger input (Pin 3, connector P3) located on the mother board. The source of counter 5 is selected as F5, a 100 Hz. square wave. Counter 5 counts from an initial value of 0099 down to 0000 which takes exactly one second since it is set up for BCD count. At 0000, OUT 5 goes active, triggering a conversion of the input at channel 0. The counter then automatically reloads itself with a 0099 and starts the process over.

BASIC:

		HEX	
10	OUT(30)=23	17	Set Data Pointer to Master Mode Register
20	OUT(28)=255	FF	Set Master Mode Register to: BCD Scaler, Data Pointer Increment
30	OUT(28)=138	8A	
40	OUT(30)=05	05	Set Data Pointer to Counter Mode Register 5
50	OUT(28)=49	31	Set Counter Mode Register 5 to: Source=F5, Reload from Load, BCD
60	OUT(28)=31	1F	Count, Active HI TC, Count Down
70	OUT(28)=153	99	Set Load Register 5 to 0099
80	OUT(28)=00	00	
90	OUT(30)=112	70	Load and Arm Counter 5
100	OUT(18)=00	00	Set Channel to 0
110	OUT(16)=12	0C	Enable External Trigger Input
300	IF IN(16)/128=0 GOTO 300		Wait for "DONE" bit
310	A=IN(18)		INPUT and PRINT Lo and Hi byte of Value just Converted
320	B=IN(20)		
330	PRINT#%,B,A		
340	GOTO 300		Go Back and Wait for Another

ASSEMBLY language Programs follow.

These programs are similar to the BASIC programs previously described.

The following routines will demonstrate how to:

1. Set up the AD212 board for time-of-day operation
2. Input and save the current time-of-day
3. Set up the AD212 board for use of alarm registers
4. Set up the AD212 board for event counting
5. Input data from a single A/D channel and save the result
6. Set up the AD212 board for auto-incrementing of the A/D converter

```
                        TITLE 'AD-200 Assembly Language Examples'

                ;
                ;               COPYRIGHT (C) 1980
                ;               TECMAR INC., BEECHWOOD, OHIO
                ;
                ;                       20-DECEMBER-1980
                ;
                ;*****************************************************************
                ;
0010 =          BASE    EQU     10H             ;BASE I/O PORT
0010 =          CMD     EQU     BASE            ;BOARD COMMAND PORT
0010 =          STAT    EQU     BASE            ;BOARD STATUS PORT
0012 =          MUX     EQU     BASE+2          ;A/D MULTIPLEXER PORT
0012 =          ADLOW   EQU     BASE+2          ;LOW BYTE OF A/D
0014 =          ADHIGH  EQU     BASE+4          ;HIGH BYTE OF A/D
0014 =          CVRT    EQU     BASE+4          ;START A/D CONVERT
001C =          DATA    EQU     BASE+12         ;9513 DATA PORT
001E =          STATUS  EQU     BASE+14         ;9513 STATUS PORT
001E =          COMMAND EQU     BASE+14         ;9513 COMMAND PORT
                ;
                ;*****************************************************************
                ;
                ; NAME:         SETTOD
                ;
                ; PURPOSE:      THIS ROUTINE SETS UP THE AD-200 BOARD
                ;               FOR TIME OF DAY OPERATION
                ;
                ; INPUT:        THE INITIAL TIME DATA MUST BE SET (IN
                ;               BCD FORMAT) IN MEMORY LOCATIONS:
                ;                       TENTH$HUND$SECS
                ;                       TENS$ONES$SECS
                ;                       TENS$ONES$MINS
                ;                       TENS$ONES$HRS
                ;                       TENS$ONES$DAYS
                ;                       THOU$HUND$DAYS
                ;
                ; OUTPUT:       AD-200 BOARD SET FOR TIME OF DAY OPERATION
                ;
                ; OTHER:        NONE
                ;
                ; SUBROUTINES
                ;       USED:   NONE
                ;
                ; NOTES:        NONE
                ;
                ;*****************************************************************
                ;

0100                    ORG     100H

                SETTOD:
0100 3EFF               MVI     A,0FFH          ;RESET MASTER MODE
0102 D31E               OUT     COMMAND

0104 3E17               MVI     A,17H           ;DATA PNTR IS MASTER MODE REG
```

```
0106 D31E               OUT     COMMAND

0108 3EFF               MVI     A,0FFH          ;SET MASTER MODE REG TO:
010A D31C               OUT     DATA            ;  BCD, INCR DATA PNTR,
010C 3E8A               MVI     A,8AH           ;  8 BIT BUS, FOUT ON,
010E D31C               OUT     DATA            ;  FOUT/10, FOUT SOURCE F5
                                                ;  COMPARE 1 & 2 ENABLED,
                                                ;  TOD ENABLED / 10

0110 3E01               MVI     A,01H           ;DATA PNTR = COUNTER MODE REG 1
0112 D31E               OUT     COMMAND
0114 3E39               MVI     A,39H           ;COUNTER MODE IS:
0116 D31C               OUT     DATA            ;  SOURCE F5, ACTIVE HI TC, BCD,
                                                ;  COUNT UP

0118 3A2602             LDA     TENTH&HUND&SECS ;LOAD TENTHS AND HUNDRETHS OF SECS
011B D31C               OUT     DATA
011D 3A2702             LDA     TENS&ONES&SECS  ;LOAD TENS AND ONES SECS
0120 D31C               OUT     DATA

0122 3E02               MVI     A,02H           ;DATA PNTR = COUNTER MODE REG 2
0124 D31E               OUT     COMMAND
0126 3E3D               MVI     A,3DH           ;COUNTER MODE IS:
0128 D31C               OUT     DATA            ;  SOURCE TC1, ACTIVE LO TC, BCD,
                                                ;  COUNT UP

012A 3A2802             LDA     TENS&ONES&MINS  ;LOAD TENS AND ONES MINUTES
012D D31C               OUT     DATA
012F 3A2902             LDA     TENS&ONES&HRS   ;LOAD TENS AND ONES HOURS
0132 D31C               OUT     DATA

0134 3E03               MVI     A,03H           ;DATA PNTR = COUNTER MODE REG 3
0136 D31E               OUT     COMMAND
0138 3E39               MVI     A,39H           ;COUNTER MODE IS:
013A D31C               OUT     DATA            ;  SOURCE TC2, ACTIVE HI TC, BCD,
                                                ;  COUNT UP

013C 3A2A02             LDA     TENS&ONES&DAYS
013F D31C               OUT     DATA
0141 3A2B02             LDA     THOU&HUND&DAYS
0144 D31C               OUT     DATA

0146 3E43               MVI     A,43H           ;COUNTERS 1,2 GET CONTENTS OF
0148 D31E               OUT     COMMAND         ;  LOAD REGISTERS

014A 3E09               MVI     A,09H           ;LOAD REG OF COUNTER 1 = ZERO
014C D31E               OUT     COMMAND
014E 3E00               MVI     A,00H
0150 D31C               OUT     DATA
0152 D31C               OUT     DATA

0154 3E0A               MVI     A,0AH           ;LOAD REG OF COUNTER 2 = ZERO
0156 D31E               OUT     COMMAND
0158 3E00               MVI     A,00H
015A D31C               OUT     DATA
015C D31C               OUT     DATA
```

```
015E 3E44               MVI     A,44H           ;LOAD COUNTER 3 FROM LOAD REG
0160 D31E               OUT     COMMAND

0162 3E27               MVI     A,27H           ;ARM COUNTERS 1, 2, 3
0164 D31E               OUT     COMMAND

0166 C9                 RET

                        PAGE
```

```
                ;*****************************************************************
                ;
                ; NAME:         GETTOD
                ;
                ; PURPOSE:      INPUT AND SAVE THE CURRENT TIME OF DAY
                ;
                ; INPUT:        FROM AD-200 BOARD
                ;
                ; OUTPUT:       CURRENT TOD SAVED IN LOCATIONS
                ;                       TENTH$HUND$SECS
                ;                       TENS$ONES$SECS
                ;                       TENS$ONES$MINS
                ;                       TENS$ONES$HRS
                ;                       TENS$ONES$DAYS
                ;                       THOU$HUND$DAYS
                ;
                ; OTHER:        NONE
                ;
                ; SUBROUTINES
                ;       USED:   NONE
                ;
                ; NOTES:        NONE
                ;
                ;*****************************************************************
                ;
                GETTOD:
0167 3EA7               MVI     A,0A7H          ;SAVE COUNTERS 1,2,3
0169 D31E               OUT     COMMAND

016B 3E11               MVI     A,11H           ;DATA PNTR = COUNTER 1 HOLD REG
016D D31E               OUT     COMMAND

016F DB1C               IN      DATA
0171 322602             STA     TENTH$HUND$SECS
0174 DB1C               IN      DATA
0176 322702             STA     TENS$ONES$SECS
0179 FE00               CPI     0               ;CHECK FOR POSSIBLE RIPPLE
017B CA8601             JZ      POSSIBLE$RIPPLE ;  ERROR
017E 3A2602             LDA     TENTH$HUND$SECS
0181 FE00               CPI     0
0183 C28A01             JNZ     NO$RIPPLE

                POSSIBLE$RIPPLE:
0186 3EA6               MVI     A,0A6H          ;IF ERROR POSSIBLE, RESAVE
0188 D31E               OUT     COMMAND         ;  COUNTERS 2,3

                NO$RIPPLE:
018A 3E12               MVI     A,12H           ;DATA PNTR = COUNTER 2 HOLD REG
018C D31E               OUT     COMMAND

018E DB1C               IN      DATA
0190 322802             STA     TENS$ONES$MINS
0193 DB1C               IN      DATA
0195 322902             STA     TENS$ONES$HRS
```

```
0198 3E13               MVI     A,13H           ;DATA PNTR = COUNTER 3 HOLD REG
019A D31E               OUT     COMMAND

019C DB1C               IN      DATA
019E 322A02             STA     TENS$ONES$DAYS
01A1 DB1C               IN      DATA
01A3 322B02             STA     THOU$HUND$DAYS

01A6 C9                 RET
                        PAGE
```

```
                ;*****************************************************************
                ;
                ; NAME:         ALARM
                ;
                ; PURPOSE:      SET UP AD200 BOARD FOR USE OF ALARM REGISTERS
                ;
                ; INPUT:        TIME FOR ALARM IS SAVED IN LOCATIONS:
                ;                       ALARM$MINS
                ;                       ALARM$HRS
                ;               IN BCD FORMAT AS ABOVE
                ;
                ; OUTPUT:       ALARM REGISTERS SET
                ;
                ; OTHER:        NONE
                ;
                ; SUBROUTINES
                ;       USED:   NONE
                ;
                ; NOTES:        THE AM09513 CONTAINS TWO 16 BIT ALARM REGISTERS
                ;               WHICH ARE CONSTANTLY COMPARED WITH COUNTER REGISTERS
                ;               1 AND 2.  WHEN ENABLED, THE OUTPUT OF THE COMPARATORS
                ;               TAKE THE PLACE OF THE NORMAL OUTPUTS OF THE COUNTERS,
                ;               OUT1 AND OUT2.  THE ACTIVE LEVEL IS DETERMINED BY THE
                ;               SETTING OF THE THE OUTPUT CONTROL, SPECIFIED IN BITS
                ;               0, 1 AND 2 OF THE INDIVIDUAL COUNTER MODE REGISTERS.
                ;               COMPARATORS 1 AND 2 ARE ENABLED BY A 1 IN BITS 2 AND 3
                ;               RESPECTIVELY IN THE MASTER MODE REGISTER.  IN THE
                ;               SPECIAL CASE THAT BOTH COMPARATORS ARE ENABLED AND THE
                ;               TIME OF DAY FUNCTION HAS BEEN ED, OUT2 WILL BE THE OUTPUT
                ;               OF A FULL 32 BIT COMPARISON OF BOTH ALARM REGISTERS
                ;               WITH THEIR RESPECTIVE COUNTERS.
                ;
                ;               THIS ROUTINE SETS UP ALARM 2 FOR A COMPARSION OF
                ;               HOURS AND MINUTES ONLY
                ;
                ;*****************************************************************
                ;
                ALARM:
01A7 3E17               MVI     A,17H           ;DATA PNTR = MASTER MODE REG
01A9 D31E               OUT     COMMAND

01AB 3EFB               MVI     A,0FBH          ;MASTER MODE REG IS:
01AD D31C               OUT     DATA            ;  COMPARATOR 1 DISABLE
                                                ;  COMPARATOR 2 ENABLE
01AF 3E0F               MVI     A,0FH           ;DATA PNTR = ALARM 2 REG

01B1 3A2C02             LDA     ALARM$MINS
01B4 D31C               OUT     DATA
01B6 3A2D02             LDA     ALARM$HRS
01B9 D31C               OUT     DATA

01BB C9                 RET
                        PAGE
```

```
                ;*****************************************************************
                ;
                ; NAME:         EVENT
                ;
                ; PURPOSE:      SET UP THE AD200 BOARD FOR EVENT COUNTING
                ;
                ; INPUT:        NONE
                ;
                ; OUTPUT:       BOARD SET FOR EVENT COUNTING
                ;
                ; OTHER:        NONE
                ;
                ; SUBROUTINES
                ;       USED:   NONE
                ;
                ; NOTES:        COUNTER 4 OF THE TIMER IS SET TO COUNT RISING
                ;               EDGES OF THE DATA COMMING IN ON SRC1
                ;
                ;*****************************************************************
                ;
                EVENT:
01BC 3EC8               MVI     A,0C8H          ;DISARM COUNTER 4
01BE D31E               OUT     COMMAND

01C0 3E04               MVI     A,04H           ;DATA PNTR = COUNTER 4 MODE REG
01C2 D31E               OUT     COMMAND

01C4 3E29               MVI     A,29H           ;COUNTER MODE 4 IS:
01C6 D31C               OUT     DATA            ;  COUNT ON RISING EDGE, SOURCE = SRC1
                                                ;  BINARY COUNT, COUNT UP
01C8 3E01               MVI     A,01H
01CA D31C               OUT     DATA
01CC 3E00               MVI     A,00H           ;LOAD REG COUNTER 4 = ZERO
01CE D31C               OUT     DATA
01D0 D31C               OUT     DATA

01D2 3E48               MVI     A,48H           ;LOAD COUNTER 4 WITH LOAD REG
01D4 D31E               OUT     COMMAND

01D6 3E28               MVI     A,28H           ;ARM COUNTER
01D8 D31E               OUT     COMMAND

01DA C9                 RET
                        PAGE
```

```
                ;*****************************************************************
                ;
                ; NAME:         SIMPLEATOD
                ;
                ; PURPOSE:      INPUT DATA FROM A SINGLE A/D CHANNEL AND
                ;               SAVE THE RESULT
                ;
                ; INPUT:        NONE
                ;
                ; OUTPUT:       DATA FROM A/D CHANNEL 0 IS SAVED IN LOCATIONS:
                ;                       LOW$BYTE
                ;                       HIGH$BYTE
                ;
                ; OTHER:        NONE
                ;
                ; SUBROUTINES
                ;       USED:   NONE
                ;
                ; NOTES:        NONE
                ;
                ;*****************************************************************
                ;
                SIMPLEATOD:
0208 3E04               MVI     A,04H           ;SET BOARD FOR LOAD ENABLE
020A D310               OUT     CMD             ; NO AUTO INCREMENT

020C 3E00               MVI     A,00H           ;SET A/D MUX FOR CHANNEL 0
020E D312               OUT     MUX

0210 D314               OUT     CVRT            ;START CONVERT

                DLOOP:
0212 DB10               IN      STAT            ;GET A/D STATUS
0214 E680               ANI     80H             ;MASK OUT DONE BIT
0216 FE00               CPI     0               ;DONE?
0218 CA1202             JZ      DLOOP           ; IF NOT, LOOP

021B DB12               IN      ADLOW           ;GET LO BYTE FIRST
021D 322E02             STA     LOW$BYTE
0220 DB14               IN      ADHIGH          ;THEN HIGH BYTE
0222 322F02             STA     HIGH$BYTE

0225 C9                 RET
                        PAGE
```

```
                ;;;
```

```
                ;*****************************************************************
                ;
                ; NAME:         AUTOATOD
                ;
                ; PURPOSE:      SET UP THE AD200 BOARD FOR AUTO TRIGGERING OF
                ;               THE A/D CONVERTER.
                ;
                ; INPUT:        NONE
                ;
                ; OUTPUT:       NONE
                ;
                ; OTHER:        NONE
                ;
                ; SUBROUTINES
                ;       USED:   NONE
                ;
                ; NOTES:        COUNTER 5 IS SET TO ISSUE A PULSE ONCE EVERY
                ;               SECOND.  A JUMPER MUST BE INSTALLED BETWEEN
                ;               OUT-5 (PIN 4, CONNECTOR P3), AND THE
                ;               EXTERNAL TRIGGER INPUT (PIN 3, CONNECTOR P3)
                ;               LOCATED ON THE MOTHER BOARD.  WITH THIS DONE,
                ;               THE A/D CONVERTER WILL START CONVERT EACH TIME
                ;               COUNTER 5 PULSES.
                ;
                ;               THE SOURCE OF COUNTER 5 IS SET TO F5, A 100HZ
                ;               SQUARE WAVE.  THE COUNTER COUNTS DOWN FROM AN
                ;               INITIAL VALUE OF 99H IN BCD MODE.
                ;
                ;*****************************************************************
                ;
                AUTOATOD:
01D8 3E17               MVI     A,17H           ;DATA PNTR = MASTER MODE REG
01DA D31E               OUT     COMMAND

01DC 3EFF               MVI     A,0FFH          ;MASTER MODE REG IS:
01DE D31C               OUT     DATA            ;  BCD, INCR DATA PNTR
01E0 3E8A               MVI     A,8AH
01E2 D31C               OUT     DATA

01E4 3E05               MVI     A,05H           ;DATA PNTR = COUNTER MODE REG 5
01E6 D31E               OUT     COMMAND

01E8 3E31               MVI     A,31H           ;COOUNTER MODE REG 5 IS:
01EA D31C               OUT     DATA            ;  SOURCE F5, AUTO RELOAD,
01EC 3E1F               MVI     A,1FH           ;  BCD COUNT, ACTIVE HI TC,
01EE D31C               OUT     DATA            ;  COUNT DOWN

01F0 3E99               MVI     A,99H           ;SET INITIAL COUNT
01F2 D31C               OUT     DATA            ;  TO 99
01F4 3E00               MVI     A,00H
01F6 D31C               OUT     DATA

01F8 3E70               MVI     A,70H           ;LOAD AND ARM COUNTER 5
01FA D31E               OUT     COMMAND
```

```
01FF 3E00               MVI     A,00H           ;SET A/D MUX ADDR TO CHANNEL
0201 D312               OUT     MUX             ;  0

0203 3E0C               MVI     A,0CH           ;ENABLE EXTERNAL TRIGGER INPUT
0205 D310               OUT     CH0

0207 C9                 RET
                        PAGE
```

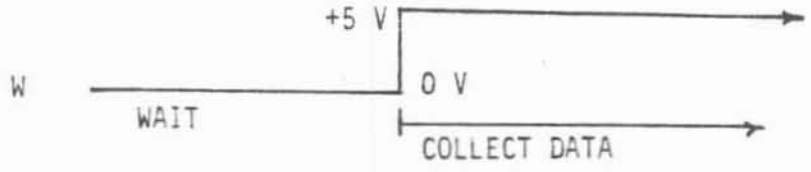
APPLICATION NOTE 1:OPERATION OF THE AD231 EXPANDER BOARDS IN THE FREE—RUN MODE

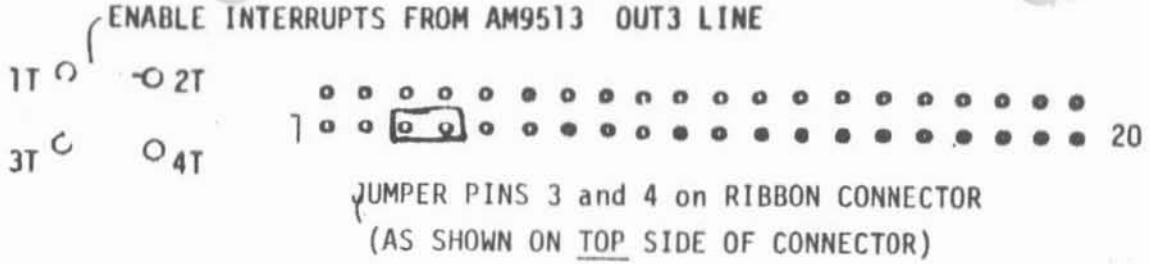
Although the AD212, Rev.C is not designed to function in the free-run mode, the addition of a simple wire wrap jumper can enable this mode. The wire wrap jumper should be connected between pin 5 and pin 8 of jumper area C on the daughter board. Jumpers between 8C and 9C and between 5C and 17C are removed and a jumper is added between 19C and 20C. All other jumpering and other considerations are the same as for the free-run mode when using an expander.

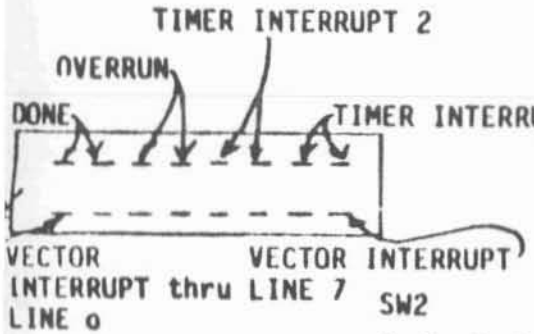
APPENDIX A

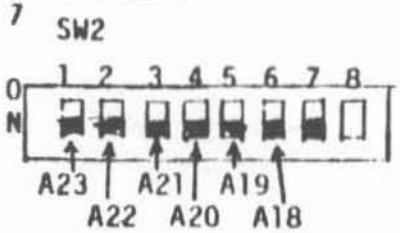
DESCRIPTION OF HOOKUP FOR EXTERNAL TRIGGER

THE EXTERNAL TRIGGER MUST PROVIDE A CONSTANT LEVEL:

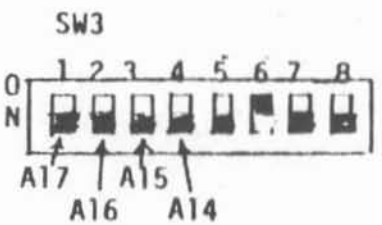




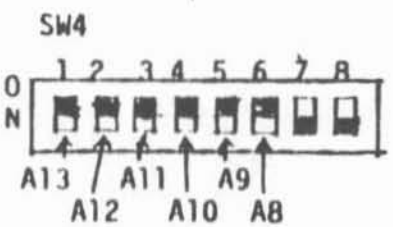




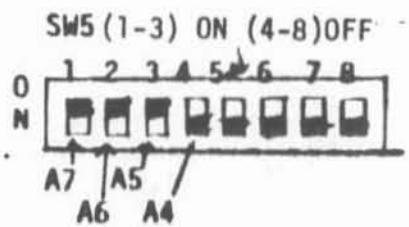
SW2 (1- 8) OFF

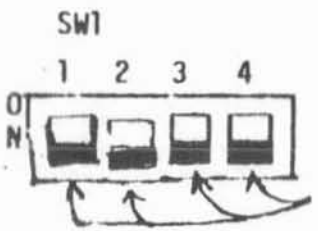


SW3 (1-5) OFF SW3 (6) ON
SW3 (7-8) OFF



SW4 (1-6) ON, SW4 (7-8) OFF





darkened portion of each switch is depressed

		SW5-5 ON	SW5-5 OFF
SW1-3,4	SINP + SOUT	MEMORY MAPPED	I/O MAPPED
	SMEMR + SMEMW	DO NOT USE	MEMORY MAPPED

APPENDIX B - AD212 MOTHER BOARD SWITCH ASSIGNMENTS

13.000 INPUT RANGE PARAMETERS

CHART OF INPUT RANGE PARAMETERS

INPUT RANGE	GAIN	** REXT (Ω)	CEXT	AMP SETTLING TIME	SYSTEM ACCURACY	*** THROUGHPUT
±10MV	1000	20.02	0.015UF	250US	±0.1%	3.8KHZ
±25MV	400	50.13	6800PF	120US	±0.08%	7.5KHZ
±50MV	200	100.5	3300PF	70US	±0.7%	12KHZ
±100MV	100	202.0	1500PF	40US	±.05%	20KHZ
±1.0 VOLT	10	2222	NONE	15US	±.03%	40KHZ
±2.5 VOLTS	4	6667	NONE	15US	±.03%	40KHZ
±5.0 VOLTS	2	20.0K	NONE	15US	±.03%	40KHZ
±10.0 VOLTS	1	NONE	NONE	15US	±.03%	40KHZ

* WITH A/D SET UP FOR BIPOLAR OPERATION I.E. 13U TO 14U
  14L TO 15L
  FOR UNIPOLAR OPERATION TIE 13U TO 14U AND 14L

** $R_{EXT} = 20000/(G-1)$

***THROUGHPUT TIME = AMPLIFIER SETTLING TIME + A/D CONVERSION TIME

250 + 10 = 260US = 3.8K CHANNELS/SEC
120 + 10 = 130US = 7.5KHZ
70 + 10 = 80US = 12KHZ
40 + 10 = 50US = 20KHZ
15 + 10 = 25US = 40KHZ

CHART OF INPUT RANGE PARAMETERS

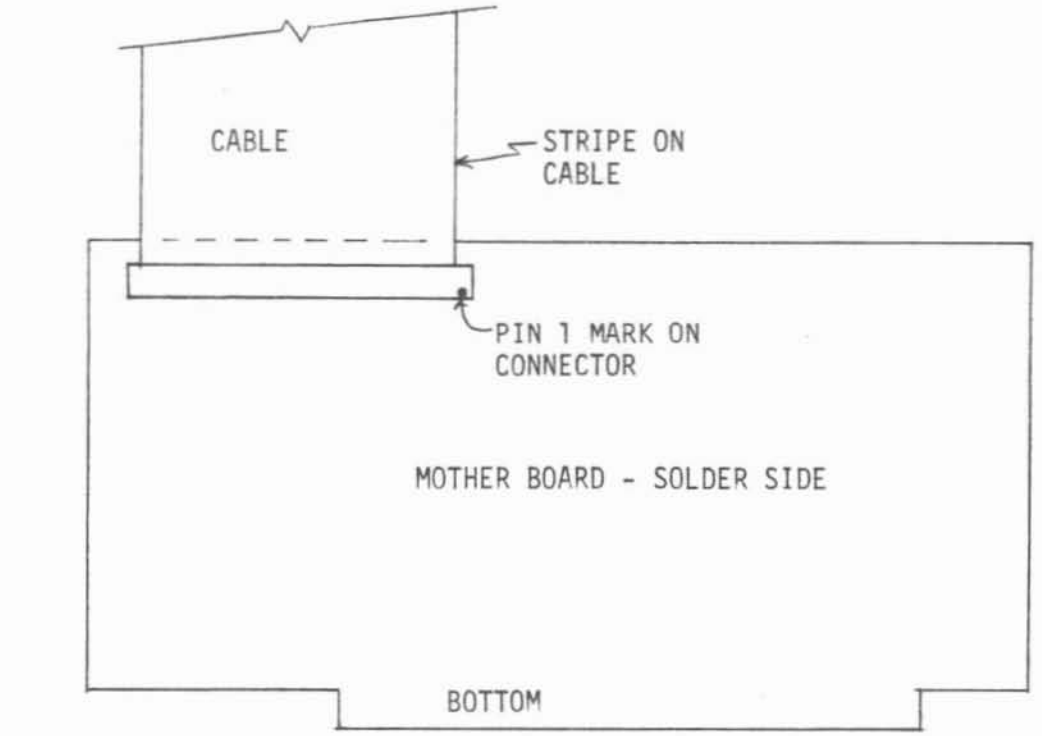
INPUT RANGE				Cext (in uF)		AMPLIFIER SETTLING TIME (in Millisec)		SYSTEM ACCURACY		THROUGHPUT RATE (in Hz)	
Unipolar	Bipolar	GAIN	Rext (in Ohms)	DT5716	DT5714	DT5716	DT5714	DT5716	DT5714	DT5716	DT5714
0 to +5mV	±5mV	2000	50.02	0.470	0.100	24.0	6.0	±.13%	±.14%	40	166
0 to +10mV	±10mV	1000	100.10*	0.220	0.056	12.0	3.0	±.06%	±.08%	80	333
0 to +25mV	±25mV	400	250.62*	0.082	0.022	4.8	1.2	±.035%	±.040%	200	833
0 to +50mV	±50mV	200	502.51*	0.039	0.010	2.4	.6	±.020%	±.022%	400	1600
0 to 100mV	±100mV	100	1,010.1*	.022	0.0047	1.2	.3	±.010%	±.020%	800	3300
0 to +1V	±1V	10	11,111*	None	None	.3	.07	±.010%	±.015%	2500	10,000
0 to +2.5V	±2.5V	4	33,333*	None	None	.3	.07	±.010%	±.012%	2500	10,000
0 to +5V	±5V	2	100,000*	None	None	.3	.07	±.009%	±.01%	2500	10,000
0 to +10V	±10V	1	NONE	None	None	.3	.07	±.0075%	±.01%	2500	10,000

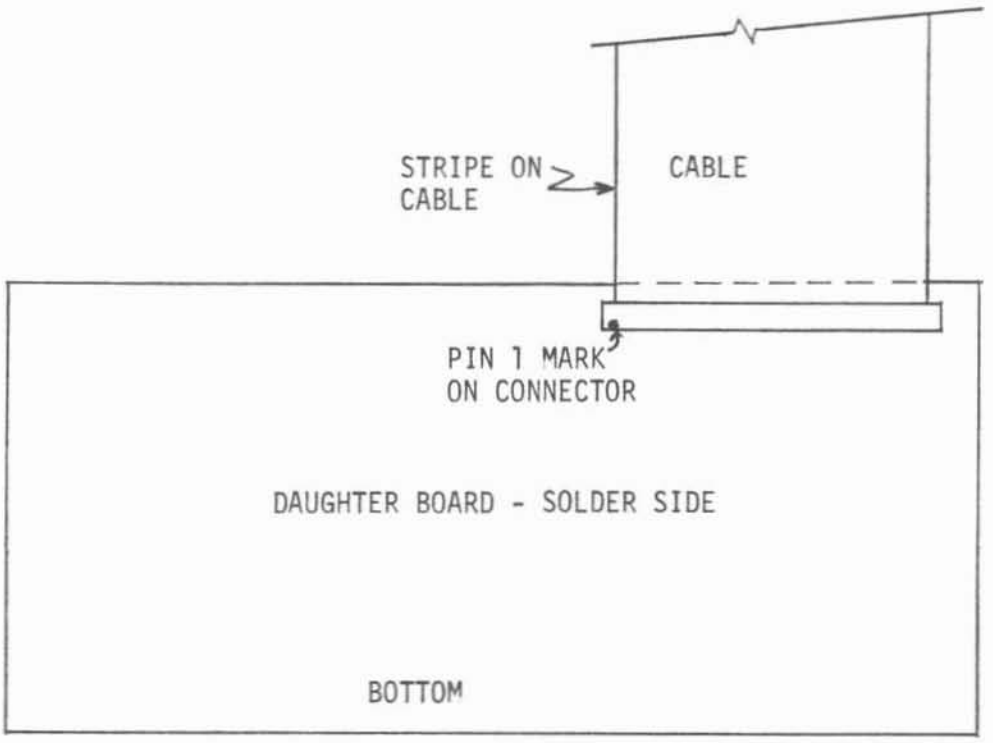
* These resistors are offered as a Precision Resistor Gain Selection Kit, Model number DT13-10501-4, for high accuracy gain setting.

$$\text{Throughput Time} = \frac{1}{\text{Amplifier Settling Time} + \text{A/D Conversion Time}} \qquad R_{EXT} = \frac{100{,}000}{(G-1)}$$

DT5714 and DT5716

APPENDIX C





CABLING BETWEEN MOTHER AND DAUGHTER BOARDS